# Exhibit 4

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 1                UNITED STATES DISTRICT COURT
 2              FOR THE EASTERN DISTRICT OF TEXAS
 3                     MARSHALL DIVISION
 4                        ---oOo---
 5    NETLIST, INC.,                )
                                    )
 6            Plaintiff.            )
                                    )
 7    vs.                           ) No. 2:22-cv-293-JRG
                                    )
 8    SAMSUNG ELECTRONICS CO,       )
      LTD; SAMSUNG ELECTRONICS      )
 9    AMERICA, INC.; SAMSUNG        )
      SEMICONDUCTOR INC.,           )
10                                  )
              Defendants.           )
11    _____  )
                                    )
12    NETLIST, INC.,                )
                                    )
13            Plaintiff.            )
                                    )
14    vs.                           ) No. 2:22-cv-294-JRG
                                    )
15    MICRON TECHNOLOGY, INC.;      )
      MICRON SEMICONDUCTOR          )
16    PRODUCTS, INC.; MICRON        )
      TECHNOLOGY TEXAS LLC,         )
17                                  )
              Defendants.           )
18    _____  )
19          VIDEOTAPED DEPOSITION OF HAROLD S. STONE, Ph.D.
20                   REMOTE PROCEEDINGS
21                 FRIDAY, AUGUST 18, 2023
22
23    STENOGRAPHICALLY REPORTED BY:
24    ANDREA M. IGNACIO, CSR, RPR, CRR, CCRR, CLR ~ CSR
      LICENSE NO. 9830
25    JOB NO. 6045577
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Page 1

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 2
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11
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20
21
22
23
24
25
                                        Page 2
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 1            I N D E X
 2
 3  WITNESS:  HAROLD S. STONE, Ph.D.
 4
 5
 6  EXAMINATION                    PAGE
 7  BY MR. SHEASBY                 7
 8
 9         ---oOo---
10
11        E X H I B I T S
12  EXHIBIT                        PAGE
13  Exhibit 1   U.S. Patent 7,619,912       19
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17  Exhibit 10  logic gate (AND, OR, XOR, NOT,   7
18         NAND, NOR and XNOR)
19  Exhibit 12  U.S. Patent 9,858,215       82
20  Exhibit 2058 FAQs Bank versus Rank      22
21
22         ---oOo---
23
24
25
                                        Page 4
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 1  A P P E A R A N C E S :
 2
 3
 4    FOR DEFENDANT SAMSUNG:
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12
13    ALSO PRESENT:  Tony Nokes, Videographer
14          George Libbares, Concierge
15
16         ---oOo---
17
18
19
20
21
22
23
24
25
                                        Page 3
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 1         REMOTE DEPOSITION PROCEEDINGS
 2            9:00 A.M.
 3            ---oOo---
 4
 5     THE VIDEOGRAPHER:  Good morning.  We are    09:01
 6  going on the record at 9:01 a.m. on August 18, 2023.   09:01
 7     Please note that this deposition is being    09:01
 8  conducted virtually.  Quality of recording depends on  09:02
 9  the quality of camera and Internet connection of    09:02
10  participants.  What is seen and heard from the witness  09:02
11  on screen is what will be recorded.            09:02
12     Audio and video recording will continue to    09:02
13  take place unless all parties agree to go off the    09:02
14  record.                          09:02
15     This is Media Unit 1 of the video-recorded    09:02
16  deposition of Dr. Harold Stone taken by counsel for   09:02
17  the Plaintiff in the matter of Netlist, Inc. versus   09:02
18  Micron Technology, Inc. et al., filed in the United   09:02
19  States District Court For the Eastern District of    09:02
20  Texas, Marshall District.  Case No.            09:02
21  2:22-CV-293-JRG-RSP                    09:02
22     This deposition is being conducted remotely.   09:02
23  The witness is appearing from Kirkland, Washington.   09:02
24     My name is Tony Nokes.  I am the          09:03
25  videographer.  The court reporter is Andrea Ignacio.  09:03
                                        Page 5
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2 (Pages 2 - 5)

1 We're here from the firm Veritext Legal Solutions.  09:03
2    I am not related to any party in this action,  09:03
3 nor am I financially interested in the outcome.  If  09:03
4 there are any objections to proceeding, please state  09:03
5 them at the time of your appearance.  09:03
6    Counsel and all present will now state their  09:03
7 appearance and affiliations for the record, beginning  09:03
8 with the noticing attorney.  09:03
9    MR. SHEASBY:  Jason Sheasby for Plaintiff.  09:03
10    MR. RUECKHEIM:  Michael Rueckheim of  09:03
11 Winston & Strawn for the Micron Defendants.  And with  09:03
12 me is Counsel James Lin, also Winston & Strawn.  09:03
13    THE VIDEOGRAPHER:  Thank you.  09:03
14    MR. DRYER:  Chris Dryer of Fish & Richardson,  09:03
15 on behalf of the Samsung witnesses.  09:03
16    THE VIDEOGRAPHER:  Thank you.  09:03
17    We may continue.  09:03
18    Will the court reporter please swear in the  09:03
19 witness.  09:03
20
21    HAROLD S. STONE, Ph.D.,
22    having been sworn as a witness,
23    by the Certified Shorthand Reporter,
24    testified as follows:
25
                                        Page 6

1    EXAMINATION
2 BY MR. SHEASBY:
3    Q   Good morning, sir.  09:04
4    Can you state your full name for the record.  09:04
5    A   My name is Harold Stuart Stone.  09:04
6    Q   And who are you -- who are you representing  09:04
7 in this matter?  09:04
8    A   I am representing Micron.  09:04
9    Q   And you've been asked to serve as an expert  09:04
10 witness for Micron -- Micron; is that correct?  09:04
11    A   That's correct.  09:04
12    Q   And your expert -- and the expert witness is  09:04
13 on sort of the plain and ordinary meaning of certain  09:04
14 terms in the specifications of the Netlist patents; is  09:04
15 that correct?  09:04
16    A   I believe that's correct.  I didn't catch the  09:04
17 beginning of your statement.  Can you repeat, please.  09:04
18    Q   Sure.  09:04
19    You've been asked to opine on what a person  09:04
20 of ordinary skill in the art would understand certain  09:04
21 terms in the Netlist patent to mean; is that correct?  09:04
22    A   That is correct.  09:05
23    (Document remotely marked Exhibit 10  09:05
24    for identification.)  09:05
25    MR. SHEASBY:  Q.  I'd like you to look at  09:05
                                        Page 7

1 Exhibit 10.  09:05
2    A   I didn't hear that.  09:05
3    Q   I'd like you to look at Exhibit 10.  09:05
4    A   You're what -- I'm sorry.  You're -- you're  09:05
5 breaking up on my audio.  You're asking me to do what?  09:05
6    Q   Look at Exhibit 10.  09:05
7    A   Oh, look at Exhibit 10.  Got it.  Okay.  I  09:05
8 will look at Exhibit 10.  09:05
9    CONCIERGE:  You'll need to either refresh  09:05
10 your browser or click on the marked folder for it to  09:05
11 come up.  09:05
12    THE WITNESS:  Yeah, I got it.  I'm now  09:05
13 opening Exhibit 10.  I'm going to download Exhibit 10.  09:05
14    So if you'll bear with me while I download,  09:06
15 I'll be ready to move on.  I -- it's coming up slowly  09:06
16 on my browser.  I thought I had downloaded it.  Let me  09:06
17 check again.  09:06
18    I apologize for taking the extra time.  Once  09:07
19 I get this set up, everything will be faster.  09:07
20    Okay.  Everything will go faster now.  It's  09:08
21 coming up on my screen.  09:08
22    I see Exhibit 10.  09:08
23    MR. SHEASBY:  Okay.  09:08
24    Q   So Exhibit 10 is just a tutorial, and there's  09:08
25 no magic of it.  I -- I literally just randomly pulled  09:08
                                        Page 8

1 one of these off the Internet last night, Dr. Stone.  09:08
2 I think there are a number of them.  09:08
3    You understand that logic has gates,  09:08
4 sometimes referred to as transistors, AND, OR, XOR,  09:08
5 NOT, NAND, NOR, and XNOR?  09:08
6    A   I am familiar --  09:08
7    MR. RUECKHEIM:  Objection to the form.  09:08
8    THE WITNESS:  Okay.  I am familiar with this.  09:08
9    MR. SHEASBY:  Q.  Are you aware of any other  09:08
10 types of gates that are used to create logic?  09:08
11    A   There may be others.  09:08
12    Q   Once in a while there's also memory gates  09:08
13 that are used to create logic; fair?  09:08
14    A   There are many different gates with -- with  09:09
15 many different representations.  These are the basic  09:09
16 ones that one would see in an introductory course.  09:09
17    Q   And you're -- there's a distinction that's  09:09
18 drawn in the art between logic circuitry and memory  09:09
19 circuitry?  09:09
20    MR. RUECKHEIM:  Object to the form.  09:09
21    THE WITNESS:  It's vague what you're asking.  09:09
22 I -- if you can clarify it, I'd be able to answer  09:09
23 that.  I'm not sure how to answer what you've asked.  09:09
24    MR. SHEASBY:  Okay.  09:09
25    Q   So I've heard of -- of -- of memory circuitry  09:09
                                        Page 9

3 (Pages 6 - 9)

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 1   before.  For instance -- for example, DRAM.        09:09
 2     A  I understand.  The -- the term "memory        09:09
 3   circuitry" may be construed in many different ways.   09:09
 4        Okay.  So you're -- your construction for      09:10
 5   memory circuitry is by giving an example of DRAM.  Now  09:10
 6   I understand what you mean.                           09:10
 7     Q  Okay.  And then there's also logic circuitry   09:10
 8   correct?                                             09:10
 9     A  You -- you're distinguishing logic circuitry   09:10
10   from memory circuitry.  I need to have you clarify   09:10
11   that for me.                                          09:10
12     Q  Tell me what clarification you need.           09:10
13     A  Well, logic may include memory circuitry, if   09:10
14   you have a broad definition of logic.  For example,   09:10
15   you can make memory out of logic.  So I'm not sure   09:10
16   what you have in mind.                                09:10
17     Q  Okay.  Do you know what logic circuitry is?   09:10
18     A  I do.                                           09:10
19     Q  What is it?                                     09:10
20     A  Logic circuitry is circuitry that performs a   09:10
21   Boolean logic.                                        09:10
22     Q  Okay.  And do you know what memory circuitry   09:10
23   is?                                                   09:11
24     A  I -- I have my own view of what memory          09:11
25   circuitry is.  I'm not sure of what your -- what your   09:11
                                                      Page 10
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 1   view is.                                             09:11
 2     Q  All right.  Give me your view.                 09:11
 3     A  My view of memory circuitry is a               09:11
 4   configuration of logic that has a state associated   09:11
 5   with it.                                              09:11
 6     Q  Okay.  And for the definition that you gave    09:11
 7   of logic, can you just restate that for me one more   09:11
 8   time so I can write it down.                          09:11
 9     A  Can you --                                      09:11
10        MR. RUECKHEIM:  Object to the form.            09:11
11        THE WITNESS:  Can you just read it off the     09:11
12   transcript?  I might not get the words right.        09:11
13        MR. SHEASBY:  Okay.                             09:11
14     Q  Well, I don't have real-time.  We'll ask --    09:11
15   it's not a test.  Give it the best you can.          09:11
16        What's the -- what's your definition of        09:11
17   logic?                                                09:11
18     A  My definition of logic -- you mean computer    09:11
19   logic?                                                09:11
20     Q  Yes.                                            09:11
21     A  Okay.  My definition of computer logic is      09:11
22   circuitry that performs Boolean operations.          09:12
23     Q  And the patents in this case are dealing       09:12
24   with -- with what would broadly be described as      09:12
25   computer logic?                                       09:12
                                                      Page 11
```

```
 1        MR. RUECKHEIM:  Object to the form.            09:12
 2        THE WITNESS:  It's -- the problem I have with   09:12
 3   answering that is that I'm not sure if you're -- if   09:12
 4   you're saying that's what it is about or if it allows   09:12
 5   for other -- other things to be in.                 09:12
 6        It's -- it's a complex case with many things   09:12
 7   in it.                                                09:12
 8        MR. SHEASBY:  It's a -- what are the other      09:12
 9   definitions of logic that you're aware of?           09:12
10        THE WITNESS:  I would -- I would have to look   09:12
11   this up to see what other people have used, what the   09:12
12   definitions are in dictionaries.  But basically,      09:12
13   computer logic are circuits that can do boolean       09:13
14   operations.                                           09:13
15     Q  And that's in contrast to sort of, like, what   09:13
16   we think of as -- as philosophical logic, for example,   09:13
17   or human logic?                                       09:13
18     A  What was the first one?  I have human logic.   09:13
19   What was the first example?                           09:13
20     Q  Philosophical logic.                            09:13
21     A  Oh, philosophic logic and human logic.         09:13
22        Well, my wife is -- is actually a logician,    09:13
23   and we have discussions we often revert back to the   09:13
24   meanings of and, or, not, because she's very good at   09:13
25   that.  So I -- I don't know how to differentiate human   09:13
                                                      Page 12
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 1   logic from what we call computer logic, except that   09:13
 2   computers do it with devices and humans do it with,    09:13
 3   yeah, intellect.                                      09:13
 4     Q  Is there a def- -- is there a different         09:13
 5   definition of computer logic in the context of memory   09:13
 6   modules?                                              09:14
 7        MR. RUECKHEIM:  Object to the form.            09:14
 8        THE WITNESS:  Well, the problem is that         09:14
 9   computer logic may have no states associated with it   09:14
10   in a particular circuit.  And then in which case I    09:14
11   would say that part of computer logic is not memory   09:14
12   logic.  But you can configure things like flip flops,   09:14
13   memory cells, and so on out of computer logic.  So    09:14
14   computer logic can encompass memory logic, and I      09:14
15   can't -- because of that, I can't quite answer your   09:14
16   question.                                             09:14
17        MR. SHEASBY:  All right.                        09:14
18     Q  Let me ask it this way:  Memory modules can    09:14
19   have computer logic on them?                          09:14
20     A  Yes, memory modules can have computer logic    09:14
21   on them.                                              09:14
22     Q  And examples of computer logic are FP- --      09:14
23   FPGAs; is that correct?                               09:15
24     A  Well, I have to ask if you're differentiating   09:15
25   computer logic from memory logic.                     09:15
                                                      Page 13
```

4 (Pages 10 - 13)

1     If you're saying is an FPGA computer logic   09:15
2  without memory logic, I cannot answer that.   09:15
3    Q  No, that's not what I'm saying.   09:15
4     I'm just saying -- so you just said there's   09:15
5  memory logic and computer logic; is that correct?   09:15
6    A  I -- I said those are terms.  I was trying to   09:15
7  figure out how you were using those terms.   09:15
8    Q  All right.   09:15
9     And you understand that programmable logic   09:15
10  devices are a type of logic -- logic; is that correct? 09:15
11    A  They are a type of logic, yes.   09:15
12    Q  And they involve both memory logic and   09:16
13  computer logic; correct?   09:16
14    A  That's correct.  They -- they have -- well,   09:16
15  the problem I have, again, is what are you talking   09:16
16  about as computer logic?   09:16
17     If you mean computer logic to be stateless   09:16
18  logic, then an FPGA has both state -- logic with state   09:16
19  and logic without state.   09:16
20    Q  All right.   09:16
21    A  That's the best I can do.   09:16
22    Q  All right.   09:16
23     And you gave me those definitions of memory   09:16
24  logic and computer logic earlier?   09:16
25    A  I -- I'm not sure I defined it for you.  I   09:16

Page 14

1  was trying to figure out what you meant.  And I -- at   09:16
2  the moment, I believe that by "computer logic," you   09:16
3  mean logic without state; and that by "memory logic,"   09:16
4  you mean logic that has state.   09:16
5    Q  All right.  And --   09:16
6    A  Go ahead.   09:16
7    Q  And a -- programmable logical devices has   09:16
8  logic with state and logic without state; correct?   09:17
9    A  That is correct.   09:17
10    Q  And so do ASICs; is that correct?   09:17
11    A  No.  Because ASICs can be anything, and so   09:17
12  they don't have to have memory with state -- logic   09:17
13  with state.  Nor do they have to have -- they can have   09:17
14  all logic with state without having any logic without   09:17
15  state.   09:17
16    I mean, I don't know.   09:17
17    Q  That's -- that's exactly my point, which is   09:17
18  that ASICs can have logic with state and/or logic   09:17
19  without state?   09:17
20    A  Is that a question?   09:17
21    Q  Yes.   09:17
22    A  The answer is yes.   09:17
23    Q  And field programmable arrays can have logic   09:17
24  with state and logic without state?   09:17
25    A  Field programmable arrays can have both.   09:18

Page 15

1    Q  Let me ask you --   09:18
2    A  Just a moment.   09:18
3     Because they're field programmable and they   09:18
4  can be -- you can make it in -- the way you'd like.   09:18
5  You may make them so that they only have logic with   09:18
6  state and they have no logic without state.  That's a   09:18
7  matter of how you construct them.   09:18
8     But because they're field programmable, they   09:18
9  have state.   09:18
10    Q  And logic encompassing both computer and   09:18
11  memory logic is created using circuit structures; is   09:18
12  that correct?   09:18
13    MR. RUECKHEIM:  Object to the form.   09:18
14    THE WITNESS:  I need you to repeat that   09:18
15  question.   09:18
16    MR. SHEASBY:  Sure.   09:18
17    Q  We talked about logic as encompassing both   09:18
18  memory logic and computer logic.   09:18
19    A  I'm sorry.  You're using the term "computer   09:18
20  logic" again.   09:18
21    Does that -- computer logic, does that have   09:18
22  state? or not state? or both?  That's what the problem 09:18
23  is for me.   09:19
24    Q  Sure.   09:19
25    Let me ask it this way:  Logic includes   09:19

Page 16

1  circuitry with state and circuitry -- circuity without 09:19
2  state?   09:19
3    A  Yes.   09:19
4    MR. RUECKHEIM:  Object to the form.   09:19
5    THE WITNESS:  Logic -- computer logictry may   09:19
6  have state and may not have state.   09:19
7    MR. SHEASBY:  Q.  And circuitry with state   09:19
8  and circuitry without state, those are actual   09:19
9  structures; right?  You can go to textbooks and look   09:19
10  those up.   09:19
11    MR. RUECKHEIM:  Object to the form.   09:19
12    THE WITNESS:  Those are actual structures.   09:19
13  I -- I believe, if you show me structures, I can   09:19
14  decide whether they have state or not.   09:19
15    MR. SHEASBY:  Okay.   09:19
16    A  If you show -- if you say this -- what is a   09:19
17  structure of -- of computer logic with state, I cannot 09:19
18  -- that's too -- too broad.  There are too many -- too 09:19
19  many different possibilities.  I don't know exactly   09:19
20  how to do that.   09:20
21    Q  No, no.  I understand that.  I'm asking it in   09:20
22  the opposite way, which is that, you can go and look   09:20
23  and physically see if the circuitry is logical   09:20
24  circuitry; circuitry with state and circuitry without 09:20
25  state?   09:20

Page 17

5 (Pages 14 - 17)

| | Page 18 | | Page 20 |
|---|---|---|---|

1    A   I can.  If -- if I have all of the          09:20

2   information available to me, I can make that          09:20

3   determination.          09:20

4    Q   Okay.  Do you know what type of products are   09:20

5   accused of infringement in this case?          09:21

6    A   I didn't get the first three words.          09:21

7       Could you repeat your question.          09:21

8    Q   Sure.          09:21

9       Do you know what types of products are          09:21

10   accused of infringement in this case?          09:21

11    A   Do I know what type of products are accused    09:21

12   of infringement in this case?          09:21

13       That's your question; is that correct?          09:21

14    Q   Yes, that's -- that's my question.          09:21

15    A   I have -- I have not studied the infringement   09:21

16   contentions.  It's only my belief that they have all   09:21

17   memory modules, but I do not -- I -- I have not          09:21

18   prepared on this.          09:21

19    Q   One second, people.  I may have lost my          09:22

20   Exhibit Share.  Yeah, it looks like I did.  Hold on.   09:22

21       Okay.  I got it back.  Give me one more          09:24

22   second.          09:24

23       Let's go to the '912 patent.          09:25

24    A   Do you have an exhibit for that, please?          09:25

25    Q   I believe the '912 patent has been marked as    09:25

Page 18

1    Q   So we're in Exhibit 1, which is the '912          09:26

2   patent; is that correct?          09:26

3    A   That's correct.          09:26

4    Q   Do you know what DDR is?          09:26

5    A   Yes, I do.          09:27

6    Q   DDR is defined by JEDEC; correct?          09:27

7    A   There are standards that involve DDR by          09:27

8   JEDEC.  The -- the original definition, I don't          09:27

9   believe it was due to JEDEC -- JEDEC.          09:27

10    Q   No.  What I'm asking is, like, at some point   09:27

11   in time, DDR became a memory that was defined by          09:27

12   JEDEC.          09:27

13    A   Let me rephrase my understanding.          09:27

14       At some point in time, JEDEC proposed a          09:27

15   standard for DDR.          09:27

16    Q   And that's -- those standard -- that standard   09:27

17   was adopted; is that correct?          09:27

18    A   I believe that's the case.  I --          09:27

19    Q   Okay.          09:27

20    A   -- did not determine that to be the case, but   09:27

21   I believe -- that's my belief.          09:27

22    Q   And at the time of the '912 patent, there was   09:27

23   a JEDEC standard adopted for -- for DDR; correct?          09:28

24    A   Well, I've not been asked to opine on          09:28

25   the '912 patent, so I haven't prepared the -- for --   09:28

Page 20

1   Exhibit 1.          09:25

2       (Document remotely marked Exhibit 1          09:25

3        for identification.)          09:25

4       MR. RUECKHEIM:  Counsel, I have Exhibit 1 as   09:25

5   Dr. Stone's declaration.          09:25

6       MR. SHEASBY:  You're in the wrong -- wrong          09:25

7   Harold Stone deposition.          09:25

8       CONCIERGE:  It should be in today's.  The          09:25

9   date is there.          09:25

10       MR. RUECKHEIM:  I don't know how to do that.   09:25

11       THE VIDEOGRAPHER:  Counsel, would you like to   09:25

12   go off the record for a moment.          09:25

13       MR. SHEASBY:  No problem.          09:25

14       THE VIDEOGRAPHER:  Thank you.  We're going          09:25

15   off --          09:25

16       MR. RUECKHEIM:  Okay.          09:25

17       THE VIDEOGRAPHER:  Thank you.  We're going          09:25

18   off the record.          09:26

19       This is the end of Media Unit 1.  The time is   09:26

20   9:26 a.m.          09:26

21       (Recess taken.)          09:26

22       THE VIDEOGRAPHER:  We are back on the record.   09:26

23       This is the beginning of Media Unit 2.  The          09:26

24   time is 9:26 a.m.          09:26

25       MR. SHEASBY:  Okay.          09:26

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1   to know its priority date and things like that.          09:28

2       Yeah, I will -- I will just say I -- I have    09:28

3   not determined if there was a DDR standard in place at  09:28

4   the time of the '912.          09:28

5    Q   All right.  So we'll just deal with one you     09:28

6   have prepared.  That will be less controversial.          09:28

7   We'll do the '215 patent, which is Exhibit 2.          09:28

8    A   Okay.  So on the '215 patent, what is your          09:28

9   question again?          09:28

10    Q   '215 patent has a priority date as of 2005,     09:28

11   if you see that.          09:28

12    A   All right.  I don't see it on the screen, but   09:28

13   I'll accept that.          09:29

14    Q   If you go to page 2.  You shouldn't accept      09:29

15   anything.  We should always dig in.          09:29

16    A   Okay.  Let me see the 2 -- the '215 patent.     09:29

17       Is that an exhibit?          09:29

18    Q   It is.  It's Exhibit 2.          09:29

19    A   Okay.          09:29

20       (Document remotely marked Exhibit 2          09:29

21        for identification.)          09:29

22       THE WITNESS:  It's coming up.  I'm going to     09:29

23   download it when I see it.  I'm downloading Exhibit 2,  09:29

24   and now I can -- I can view Exhibit 2 on my computer.   09:29

25       MR. SHEASBY:  Okay.          09:29

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6 (Pages 18 - 21)

| | |
|---|---|
| 1   Q  Why don't you go to page 2 to look at the   09:29 | 1  components."   09:34 |
| 2  date.   09:29 | 2    Q  Do you disagree with Micron's definition of   09:34 |
| 3    A  Okay.  I'm on page 2.  And it claims a   09:29 | 3  banks and ranks?   09:34 |
| 4  provisional application filed on 2005.   09:30 | 4      MR. RUECKHEIM:  Object to the form.   09:34 |
| 5      So that's presumably a claim priority date.   09:30 | 5      THE WITNESS:  I believe that many   09:34 |
| 6  I don't know if that's been accepted.   09:30 | 6  definitions -- in fact, competing and inconsistent   09:34 |
| 7    Q  I understand that.  So it's a claim priority   09:30 | 7  definitions -- exist for banks and ranks.  What I read  09:34 |
| 8  date.   09:30 | 8  here is credible.   09:34 |
| 9      You understand that JEDEC had defined what --  09:30 | 9      MR. SHEASBY:  Q.  What are the competing   09:34 |
| 10  what DDR is by that date?   09:30 | 10  definition of banks and ranks?   09:34 |
| 11    A  There was a JEDEC standard by that date for   09:30 | 11      MR. RUECKHEIM:  Objection to form.   09:35 |
| 12  DDR, yes.   09:30 | 12      THE WITNESS:  Well, one definition that I   09:35 |
| 13    Q  Okay.  But...   09:30 | 13  used in my book was for a bank.  And that's in my book  09:35 |
| 14      (Document remotely marked Exhibit 2058   09:31 | 14  on "Microcomputer Interfacing."  And I did not use   09:35 |
| 15       for identification.)   09:31 | 15  bank in the sense that banks are specific to   09:35 |
| 16      MR. SHEASBY:  Q.  Okay.  I marked a new   09:31 | 16  individual DRAM components and refer to subarrays   09:35 |
| 17  exhibit.  It's Exhibit 2058.   09:31 | 17  within the DRAM as opposed to memory modules, because  09:35 |
| 18    A  Okay.  Just a moment.   09:31 | 18  my book occurred before there were memory modules.   09:35 |
| 19      I have Exhibit 3.  Is that the one you have   09:32 | 19      And at the time I wrote the book, banks and   09:35 |
| 20  for the '417?   09:32 | 20  ranks were more or less used as terms interchangeably.  09:35 |
| 21    Q  No.  If you refresh, you'll see Exhibit 2058.   09:32 | 21  So there's an example.   09:35 |
| 22    A  Okay.  I got it.  FAQs; right?   09:32 | 22      MR. SHEASBY:  Q.  When did you write your   09:35 |
| 23      I am downloading it now.  I see the exhibit.   09:32 | 23  book?   09:35 |
| 24    Q  And this is from a Micron website.  You can   09:33 | 24    A  In 1980, first edition.   09:35 |
| 25  see that by looking in the middle of the page.   09:33 | 25    Q  And you understand that after -- that after   09:35 |
| Page 22 | Page 24 |

| | |
|---|---|
| 1    A  I see the Micron in the middle of the page,   09:33 | 1  you created your book, memory -- memory modules came   09:35 |
| 2  yes.   09:33 | 2  to existence?   09:36 |
| 3    Q  And if you scroll down, it says:   09:33 | 3      MR. RUECKHEIM:  Object to the form.   09:36 |
| 4      (As read):   09:33 | 4      THE WITNESS:  I believe that's the case, yes.  09:36 |
| 5      "What's the difference between bank and a   09:33 | 5      MR. SHEASBY:  Q.  What's a memory module?   09:36 |
| 6  rank?"   09:33 | 6    A  A memory module is a module that contains   09:36 |
| 7      Do you see that?   09:33 | 7  memory.   09:36 |
| 8    A  I see what is a rank; is that what you're   09:33 | 8    Q  That's the only requirement?   09:36 |
| 9  referring to?   09:33 | 9    A  I'm not sure why there's a requirement.   09:36 |
| 10    Q  It says:   09:33 | 10  That -- if I had a module in my hand, and I looked at   09:36 |
| 11      (As read):   09:33 | 11  it to see if it had memory, I would say, "Hey, that's   09:36 |
| 12      "What is the difference between a bank and a   09:33 | 12  a memory module."   09:36 |
| 13  rank?"   09:33 | 13      When we come to a question saying, Is this a   09:36 |
| 14      Do you see that?   09:33 | 14  standard memory module? that's a different question;   09:36 |
| 15    A  Yeah, I encountered the other one first.  So   09:33 | 15  and then you would -- and whatever is required to meet  09:36 |
| 16  shall I click on that?   09:33 | 16  the definition for that standard.   09:36 |
| 17    Q  I don't think it's active.  I think it's just   09:34 | 17      As you asked the question generically, I   09:36 |
| 18  the -- what -- what comes up is right below that.   09:34 | 18  would say a module with memory.   09:36 |
| 19    A  Okay.  May I read that?   09:34 | 19    Q  And it's not a module with memory that serves  09:36 |
| 20    Q  Yes, please.   09:34 | 20  as a doorstop; right?   09:36 |
| 21    A  (As read):   09:34 | 21      A memory module is a module with memory that   09:37 |
| 22      "Banks are specific to individual DRAM   09:34 | 22  is connectable to the computer system and can be   09:37 |
| 23  components and refer to subarrays within the DRAM   09:34 | 23  controlled by a memory controller?   09:37 |
| 24  component.  Ranks are specific to memory modules and   09:34 | 24    A  That's a module, yes.   09:37 |
| 25  refer to a subarray made of multiple DRAM   09:34 | 25    Q  Do you know of any memory modules that aren't  09:37 |
| Page 23 | Page 25 |

7 (Pages 22 - 25)

1  connected to a computer system --          09:37
2    A  Yes.                                  09:37
3    Q  What memory modules are not connectable to a   09:37
4  computer system?                           09:37
5    A  If I hold up my phone -- here.  Let me get   09:37
6  this on the screen.  I'm trying to get it on the   09:37
7  screen.  Okay.  Better.                    09:37
8      This phone has a memory module in it that I   09:37
9  installed myself.                          09:37
10   Q  You put in a memory card?             09:37
11   A  I put in a -- a small memory module.  09:37
12   Q  A memory card?                        09:37
13   A  No, it's called a module.             09:37
14   Q  What is -- what is it that you put in?   09:38
15   A  I can take it out.  Perhaps I can probably   09:38
16  show you an example of one.                09:38
17      The -- what -- it's called a microSD card.   09:38
18   Q  And that microSD card interfaces with the   09:38
19  computer processor in the chip; correct?   09:38
20   A  It does.                              09:38
21   Q  And it interfaces with a memory controller on   09:38
22  that computer processor; correct?          09:38
23   A  That is correct.                      09:38
24   Q  So like I said, memory modules interface with   09:38
25  memory controllers and computer systems, or computer   09:38

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1  processor.  Maybe that's a better way of saying it.   09:38
2    A  I just gave you an example of one that I   09:38
3  believe was not what you had intended to say.  You   09:38
4  were talking about computers, I had a phone.  So I   09:38
5  didn't know how to answer.  I think I answered   09:38
6  correctly.                                 09:39
7    Q  Let me do -- you understand that phones have   09:39
8  computer processors in them now, correct?   09:39
9    A  I do.                                 09:39
10   Q  All right.  So memory modules are modules of   09:39
11  memory that connect to computer processors and memory   09:39
12  controllers?                               09:39
13     MR. RUECKHEIM:  Object to the form.     09:39
14     THE WITNESS:  In general, but not       09:39
15  necessarily.                               09:39
16     MR. SHEASBY:  Okay.                     09:39
17   Q  Give me an example of a memory module that   09:39
18  doesn't connect to a computer processor and a memory   09:39
19  controller.                                09:39
20   A  I have in my house Kasa videos.  They have   09:39
21  memory modules in them.  Now, it's hard for me to say   09:39
22  that the Kasa camera is a computer and has a processor   09:39
23  in there.  It has something that can read and write   09:39
24  the memory module.                         09:39
25   Q  You have Kasa -- what are these things?   09:39

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1    A  I'm sorry.  Would you repeat your question.   09:39
2    Q  Kasa, are these house cameras?  Is that -- is   09:39
3  that what you're saying?                    09:39
4    A  That's correct.                       09:39
5    Q  And those house cameras have memory modules   09:39
6  in them; correct?                          09:40
7    A  They do.  I put one in.               09:40
8    Q  And those memory modules record video; is   09:40
9  that correct?                              09:40
10   A  They do.                             09:40
11   Q  And what controls when the video records and   09:40
12  doesn't record?                            09:40
13   A  A digital camera.                     09:40
14   Q  And the digital camera has a processor in it;   09:40
15  correct?                                   09:40
16   A  I believe -- it probably does.  I can't   09:40
17  confirm for sure.                          09:40
18   Q  And it has a controller for that memory;   09:40
19  correct?                                   09:40
20   A  There is something in the camera that is able   09:40
21  to process the video and place it onto the memory   09:40
22  card.                                      09:40
23   Q  What are the patents in the -- the patents in   09:40
24  the -- in this case are directed to memory modules   09:40
25  that -- that are used in servers; correct?   09:40

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1    A  I don't know their use.  I haven't studied   09:40
2  that.                                      09:40
3    Q  You don't know what the use is of the memory   09:40
4  modules in the patents-in-suit are?         09:41
5      MR. RUECKHEIM:  Object to the form.     09:41
6      THE WITNESS:  It was -- I have not reviewed   09:41
7  anything regarding the accused modules.  So I'm not   09:41
8  sure where they're used or how they're used or   09:41
9  anything like that.  I have only looked at the -- in   09:41
10  this case, the patents and some relevant information   09:41
11  about the patents.                         09:41
12     MR. SHEASBY:  Q.  So if you go down to    09:41
13  the '215 patent is says "field of invention" on   09:41
14  page 1; do you see that?                    09:41
15     THE WITNESS:  All right.  Let me do that.   09:41
16  Just a moment.  I am in the '215 patent and I'm   09:41
17  looking.  And you -- page 1?                09:41
18   Q  Yes.  Column 1, PDF page 1.            09:41
19   A  Got it.                              09:41
20   Q  It says:                             09:41
21     (As read):                            09:41
22     "Field of invention, this present invention   09:41
23  relates to..."                             09:42
24     Do you see that?                       09:42
25   A  On page 1 of the '215, the present...   09:42

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8 (Pages 26 - 29)

1    Can you advise me as to where -- it's in the    09:42
2 middle or bottom or -- I don't --    09:42
3    Q  Column 1 -- oh, left-hand side, because it's    09:42
4 not a column.    09:42
5    A  Okay.    09:42
6    Q  And -- and I think -- no, wait.  One second.    09:42
7 Now my -- my Adobe Reader has frozen.    09:42
8        Look for "Field of invention," while my    09:42
9 reader wakes itself up again.    09:42
10    A  Okay.  I'm looking for...    09:42
11    Q  It says "Background of invention."  It's on    09:42
12 page 2.    09:42
13    A  Oh, page 2.  Sorry.    09:42
14    Q  Page 2 column 1, it looks like.  "Background    09:42
15 of invention."  "Field of invention."    09:43
16    A  On page 2, I don't see "Field of the    09:43
17 Invention."    09:43
18        I see -- is it highlighted?  Is it in bold?    09:43
19    Q  One sec.  I'm going to access my Adobe    09:43
20 Acrobat and get back in.    09:43
21        So we're in Exhibit 2.  That's the '215    09:43
22 patent; correct?    09:43
23    A  That's correct.    09:43
24    Q  And if you go to -- oh, I see what the    09:43
25 problem is.    09:44

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1        Apparently my pagination had frozen.  It's    09:44
2 nowhere near page 2.    09:44
3        Go to column 1, which is on PDF page 35.    09:44
4    A  Okay.  I am on column 1.    09:44
5    Q  It says "field of the invention"; do you see    09:44
6 that?    09:44
7    A  I do.    09:44
8    Q  It says:    09:44
9        (As read):    09:44
10        "The present invention relates generally to    09:44
11 memory modules of a computer system."    09:44
12        Do you see that?    09:44
13    A  I do.    09:44
14    Q  And memory modules of computer systems can    09:44
15 connect to memory controllers on those computer    09:44
16 systems; correct?    09:45
17    A  In general, yes.    09:45
18    Q  Do you know of any memory modules for    09:45
19 computer systems that can't connect to the memory    09:45
20 controller on the computer system?    09:45
21    A  Well, I do, but that's because there are many    09:45
22 different ways you can put memory modules into a    09:45
23 computer system.  Some of them don't involve going to    09:45
24 the controller that you're referring to.  There may be    09:45
25 many memory controllers so I can't -- I can't say for    09:45

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1 certain that the controller that you have in mind can    09:45
2 connect to all of the memory modules.    09:45
3    Q  You think I was limiting it to one particular    09:45
4 memory controller?    09:45
5    A  I only heard memory controller in the    09:45
6 singular.    09:45
7    Q  Memory modules of a computer system will be    09:45
8 able to connect to a memory controller; correct?    09:46
9        MR. RUECKHEIM:  Object to the form.    09:46
10        THE WITNESS:  Are you saying that in every    09:46
11 instance, if there's a memory module in a computer    09:46
12 system, it will be able to connect to a memory    09:46
13 controller?  Is that your question?    09:46
14        MR. SHEASBY:  No.    09:46
15    Q  My question is:  In the context of -- of    09:46
16 computer systems, what are the attributes of memory    09:46
17 modules?    09:46
18        MR. RUECKHEIM:  Object to the form.    09:46
19        THE WITNESS:  Could you repeat your question.    09:46
20        MR. SHEASBY:  Sure.    09:46
21    Q  In the context of -- of computer systems,    09:46
22 what are the attributes of memory modules?    09:46
23    A  In the context of computer systems, what are    09:46
24 the attributes of memory modules?    09:46
25    Q  Yes.    09:46

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1    A  Is that your question?    09:46
2    Q  That is my question.    09:46
3    A  A memory module in a computer system can    09:47
4 store -- can store data.  I'll just leave it at that.    09:47
5    Q  And is it possible to store data without    09:47
6 being able to communicate with the computer system?    09:47
7    A  If I were charged with building such a    09:47
8 device, I could.  But I don't think that's what your    09:47
9 question pertains to.    09:47
10        So I -- your -- I can't answer your question    09:47
11 as asked because there are too many ways to respond.    09:47
12    Q  So you think that in the patents-in-suit in    09:47
13 this case it's contemplating memory modules that are    09:47
14 not interfacing with computer systems?    09:47
15        MR. RUECKHEIM:  Object to the form.    09:47
16        THE WITNESS:  I -- I believe that the modules    09:47
17 in these patents are directed to modules that can --    09:47
18 are -- are in computer systems and can interact with    09:48
19 the computer system.    09:48
20        MR. SHEASBY:  Okay.    09:48
21    Q  Now, if we go down to the claims -- and you    09:48
22 did review the claims; correct?    09:48
23    A  I did.    09:48
24    Q  And we'll just go to the '215 patent, for    09:48
25 example.    09:48

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9 (Pages 30 - 33)

Page 34

```
 1      So as of 2005, which is the filing of        09:48
 2  the '215 patent and the '417 patent, do you have an   09:48
 3  understanding of rank that is different from what     09:48
 4  Micron presented?                                      09:49
 5      MR. RUECKHEIM:  Object to the form.          09:49
 6      THE WITNESS:  I have not been asked to opine  09:49
 7  on rank and bank, or meaning of rank in this patent.  09:49
 8  So I would have to review the materials and determine  09:49
 9  what they mean by "rank" and -- and look at all the   09:49
10  information I have to make an opinion on what rank    09:49
11  means for this patent.  I have not done that.  I've   09:49
12  not been asked to do that.                            09:49
13      MR. SHEASBY:  Okay.                          09:49
14   Q  I'm just asking you, as a person of ordinary  09:49
15  skill, as of 2005, do you disagree with Micron's     09:49
16  definition of rank?                                   09:49
17      MR. RUECKHEIM:  Same objection.              09:49
18      THE WITNESS:  I believe that Micron's        09:49
19  definition is -- is compatible with many other ways to  09:49
20  define "rank" for modules.  I don't know that it was  09:49
21  unique or only or the correct one.                    09:49
22      It -- it's -- it's -- it's a credible        09:50
23  definition, but I can't opine to say that I agree or   09:50
24  disagree.                                              09:50
25      MR. SHEASBY:  All right.                     09:50
                                                    Page 34
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```
 1   Q  So you believe that Micron's definition of    09:50
 2  rank is a credible definition of rank as of the field  09:50
 3  of memory modules in 2005?                             09:50
 4   A  It is credible, yes.                          09:50
 5      MR. RUECKHEIM:  Object to the form.          09:50
 6      MR. SHEASBY:  Okay.                          09:50
 7   Q  And are you aware of any, in your experience,  09:50
 8  as of specifically as of memory modules in the -- and,  09:50
 9  by the way, you agree the patents-in-suit are directed  09:50
10  at JEDEC memory modules; correct?                      09:50
11   A  I'm sorry.  There were two questions that     09:50
12  you're asking at the same time.  And I -- I want a     09:50
13  clearer question asked.                                09:50
14   Q  All right.                                    09:50
15      You -- you agree that the patents are        09:50
16  directed at JEDEC memory modules?                      09:50
17   A  I don't know if I agree with that.  I know    09:50
18  that they're cited in there.                           09:50
19   Q  They're -- the patents are directed at        09:50
20  JEDEC-style memory modules.                            09:50
21   A  I -- I understand that they're referenced in  09:50
22  here, yes.  I don't -- they may be directed at other   09:51
23  kinds of memory modules as well.  I don't know.        09:51
24   Q  Are the patents intended to be understood by  09:51
25  folks who are familiar with the JEDEC specifications   09:51
                                                    Page 35
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```
 1  that existed at the time?                        09:51
 2   A  I believe that a person familiar with JEDEC   09:51
 3  specifications at the time will be qualified to read   09:51
 4  and understand the patent.                             09:51
 5   Q  And the -- the patents were developed with    09:51
 6  the goal of complying with JEDEC standards; correct?  09:51
 7      MR. RUECKHEIM:  Object to the form.          09:51
 8      THE WITNESS:  I don't know what the goals of  09:51
 9  the inventors were at the time.                        09:51
10      MR. SHEASBY:  Okay.                          09:51
11   Q  Well, why don't we go to your declaration.    09:51
12  I'll pull that up.                                     09:51
13   A  Okay.  Is that in the exhibits now?          09:51
14   Q  It will be shortly.  Okay.  It's been         09:51
15  uploaded.  It's Exhibit 5.  Let me know when you get   09:52
16  it.                                                    09:52
17      (Document remotely marked Exhibit 5          09:52
18       for identification.)                        09:52
19      THE WITNESS:  I see it.  I'm in the process   09:52
20  of loading it into the computer and downloading it.   09:52
21  It has reached my computer.  I'm now downloading it.   09:52
22      Okay.  And now I'm opening it on my computer.  09:53
23  I have it.                                             09:53
24      MR. SHEASBY:  Q.  And if you go to           09:53
25  paragraph 44.                                          09:53
                                                    Page 36
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```
 1      By the way, did you write your declaration?   09:53
 2   A  I did.  Well, when you say "write," obviously  09:53
 3  there's interaction what -- on -- when I sign for      09:53
 4  something, I always commit to either writing it or --  09:53
 5  or agreeing with everything that's said.               09:53
 6      Okay.  Here's 44.                            09:53
 7   Q  Go ahead and read the first two sentences.    09:53
 8   A  I should read them to you; right?             09:54
 9   Q  You can read them to yourself.               09:54
10   A  Okay.                                         09:54
11      Okay.  I have that.                          09:54
12   Q  Does this refresh your rec- -- your           09:54
13  recollection that you opined that persons of ordinary  09:54
14  skill in the art dealing with these patents would be  09:54
15  approaching them with the standpoint of being in      09:54
16  compliance with JEDEC?                                 09:54
17      MR. RUECKHEIM:  Object to the form of the     09:54
18  question.                                              09:54
19      THE WITNESS:  Yes, I -- when I -- you asked a  09:54
20  question about what was the intent of the inventors.   09:54
21  I didn't know what that was.                           09:54
22      This says that the patents -- memory          09:54
23  technology in the field was developed primarily       09:54
24  with -- with an understanding and a goal of complying  09:54
25  with the underlying standards.  Okay.                  09:54
                                                    Page 37
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10 (Pages 34 - 37)

Page 38

```
 1        MR. SHEASBY:  Yeah.                   09:54
 2     Q  So basically you agree the patents at issue    09:55
 3  in this case, a POSA would approach them with the      09:55
 4  understanding with the end goal of complying with the   09:55
 5  preexisting JEDEC standards?                 09:55
 6     A  My statement, in general, about memory       09:55
 7  technology is these patents are specific.  They may    09:55
 8  agree with what was going on, in general; but, again,  09:55
 9  I can't confirm exactly what was in the minds of the   09:55
10  inventors.                         09:55
11     Q  Yeah, I'm not talking about what is in the    09:55
12  minds of the inventors.  To a POSA, a POSA reading     09:55
13  these patents would understand them as being -- as    09:55
14  creating technology that would be compliant with JEDEC 09:55
15  standards?                         09:55
16     A  Yes, that is --                    09:55
17        MR. RUECKHEIM:  Object to the form.        09:55
18        THE WITNESS:  A POSA would believe that these  09:55
19  patents were supposed to comply with JEDEC standards.  09:56
20        MR. SHEASBY:  Okay.                 09:56
21     Q  And Micron makes products that comply with    09:56
22  JEDEC standards; correct?                  09:56
23     A  To my understanding, yes, but I have not     09:56
24  confirmed that.                      09:56
25     Q  So now let's go back to Micron's definition   09:56
```

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```
 1  of rank.                          09:56
 2     A  Okay.  I have that.                 09:56
 3     Q  And let's go to -- I'm going to add another   09:56
 4  exhibit.                          09:57
 5     A  Let's go to where?                  09:57
 6     Q  I'm going to add another exhibit.  Give me    09:57
 7  one moment.                        09:57
 8     A  Okay.                         09:57
 9        (Document remotely marked Exhibit 8        09:57
10        for identification.)                09:57
11        MR. SHEASBY:  It's Exhibit 8.  Let me know    09:57
12  when you get it and you can pull it up.          09:57
13     A  Exhibit 8 appears in my -- on my directory.   09:57
14  I've asked for it to come to the computer.  It's on    09:57
15  its way.  I see it.  I'm now going to download it to   09:57
16  my computer.  And it's on my computer and I'm going to 09:57
17  open it.                          09:58
18        Okay.  I can see it.                09:58
19     Q  And this is a doc- -- document from Micron,   09:58
20  you can see that, if you go down to the -- the last    09:58
21  page.                           09:58
22     A  Page 2; is that right?               09:58
23     Q  Yes.                         09:58
24     A  Mine is kind of messy.  I -- what am I       09:58
25  looking for?                       09:58
```

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```
 1     I see a copyright to Micron Technology.  Is     09:58
 2  that what I'm supposed to look at, the copyright?      09:58
 3     Q  Sure.                         09:58
 4     A  Okay.  I see the copyright.            09:58
 5     Q  At the top it says "What is a memory rank";   09:58
 6  do you see that?                     09:58
 7     A  Yes.                         09:58
 8     Q  It says:                       09:58
 9     (As read):                      09:58
10        "The term 'rank' was created by JEDEC, the    09:58
11  memory industry standards group, to distinguish       09:59
12  between number of memory banks in a module as to the   09:59
13  number" -- "as opposed to the number of memory banks   09:59
14  on a component or memory chip."              09:59
15     A  I see that.                     09:59
16     Q  And it says:                     09:59
17     (As read):                      09:59
18        "A memory rank is a block or area of data     09:59
19  that is created using some or all of the memory chips  09:59
20  in a module."                      09:59
21        Do you see that?                  09:59
22     A  I see that.                     09:59
23     Q  And that's consistent with the previous      09:59
24  definition of rank that we saw that Micron gave;       09:59
25  correct?                          09:59
```

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```
 1        MR. RUECKHEIM:  Object to the form.        09:59
 2        MR. SHEASBY:  Q.  This was Exhibit --       09:59
 3     A  Okay.                         10:00
 4     Q  -- 2- -- Exhibit 2058.               10:00
 5     A  I understand.  I'm looking at this.  Okay.    10:00
 6  I'm looking at that, and I'm going to correct         10:00
 7  Exhibit 2058, but I do have a problem.           10:00
 8        They are different.  The two -- the two      10:00
 9  exhibits are different.  And they -- you can combine   10:00
10  them to get something.  But I cannot say -- I don't    10:01
11  know what your question is.  But I -- all I can say is  10:01
12  that they're different.                  10:01
13     Q  Yeah.  My question is:  Are they consistent?  10:01
14        MR. RUECKHEIM:  Object to the form.        10:01
15        THE WITNESS:  Well, I can't be sure.  And    10:01
16  that depends what you do when use Exhibit 8.         10:01
17        MR. SHEASBY:  Tell me what you mean.        10:01
18     A  Banks are defined in Exhibit 2058.  Is that   10:01
19  it?  2058?                         10:01
20     Q  Uh-huh.                       10:01
21     A  Yeah.  It says what a bank is.  Banks aren't   10:01
22  defined in Exhibit 8, to my knowledge.  I'm looking at 10:01
23  it.                            10:01
24        To the best I can do, I haven't read it      10:01
25  thoroughly, I'm looking for a definition of bank.  I   10:01
```

11 (Pages 38 - 41)

```
 1  cannot find one.  If there is, please let me know.  It  10:01
 2  may be possible that bank is defined differently      10:02
 3  within the minds of whoever wrote this, and           10:02
 4  differently from Exhibit 2058.  I can't tell.  So I   10:02
 5  can't tell if it's consistent or inconsistent.        10:02
 6  It's -- it's uncertain.                               10:02
 7     Q  Okay.  Is the definition of ranks in the two    10:02
 8  documents consistent?                                 10:02
 9        MR. RUECKHEIM:  Same objection.                 10:02
10        THE WITNESS:  Since I haven't seen these        10:02
11  before, I'm trying to do the best I can.              10:02
12        MR. SHEASBY:  Q.  Well, take as much -- we      10:02
13  have seven hours, so you should take as much time as  10:02
14  you need.                                             10:02
15     A  I hope I don't use all of them, but it's not    10:02
16  easy.  And the answer is that they don't seem to be   10:02
17  consistent.  I can't be for -- say for sure.          10:03
18     Q  Why don't they seem to be consistent?          10:03
19     A  Well, I'm looking now at Exhibit 8.  I'm        10:03
20  looking at the second paragraph.  It says:            10:03
21     (As read):                                        10:03
22     "Depending on how a memory module is               10:03
23  engineered, it may have one, two, or four blocks of   10:03
24  64-bit wide areas," et cetera.                        10:03
25        And a memory rank is a block of area of data    10:03
                                                        Page 42
```

```
 1  that is created using some or all of the memory chips  10:03
 2  on a module.  According to what I read here, a memory  10:03
 3  rank can be one or two or four of the blocks.  That's  10:04
 4  not consistent with 2058, if I read it correctly, but  10:04
 5  I'm not sure.                                         10:04
 6     Q  Why isn't it consistent?                        10:04
 7     A  Ranks are -- I'm reading now to 2058.           10:04
 8     (As read):                                        10:04
 9     "Ranks are specific to memory modules and          10:04
10  refer to a subarray made of multiple DRAM             10:04
11  components."                                          10:04
12        Now, that is singular, "a subarray."  Okay?     10:04
13        So a rank is one thing, and it's a subarray.    10:04
14        Now we go to Exhibit 8.  It says that you may   10:04
15  have one four-block area and that can be -- later it   10:05
16  says this is referred to as a single rank.  That's not 10:05
17  a subarray.                                           10:05
18     Q  You don't think a one-block is a subarray?      10:05
19     A  No, if you have one block, and you only have    10:05
20  one block on the board, it's not a subarray.          10:05
21     Q  Oh, I get your point.                           10:05
22        And how many chips will you have in that one    10:05
23  block?                                                10:05
24     A  I don't know.  I mean you have 72 bits.         10:05
25     Q  Is there any system in which a single chip      10:05
                                                        Page 43
```

```
 1  can give you 72 bits, can allow for 72 --              10:05
 2     A  No, but -- no, but the chips are different       10:05
 3  widths.  You asked how many chips.  I don't know.      10:05
 4     Q  It will be a number greater than 1?              10:05
 5     A  Right now?  I don't know of any right now,       10:05
 6  but next year, maybe.                                 10:06
 7     Q  At any time in the past, it has always been a   10:06
 8  number greater than 1?                                 10:06
 9     A  Well, the problem is this is a definition of    10:06
10  memory rank for present, past, and future, and you're 10:06
11  asking me about the past only.  And I'm talking about 10:06
12  what about the future.                                10:06
13     Q  Right.  But I'm -- but you have to answer my    10:06
14  question because that's the rules.                    10:06
15        And so, in the present and past, rank has       10:06
16  always been more than one chip?                       10:06
17        MR. RUECKHEIM:  Object to the form.             10:06
18        THE WITNESS:  In the present and past for       10:06
19  this definition of rank, for this definition, it has  10:06
20  been more than one chip.                              10:06
21        MR. SHEASBY:  Okay.                             10:06
22     Q  And for rank in the context of -- of JEDEC,     10:06
23  in the present and past, there's always been more than 10:06
24  one chip?                                             10:06
25        MR. RUECKHEIM:  Object to the form.             10:06
                                                        Page 44
```

```
 1        THE WITNESS:  In the context of JEDEC, you      10:06
 2  know, there are many JEDEC standards in the past.  I   10:06
 3  haven't studied that.  I don't know.                  10:07
 4        MR. SHEASBY:  All right.                        10:07
 5     Q  As a general rule, you have some -- you         10:07
 6  consider yourself a person of skill in the art in the 10:07
 7  field of JEDEC memory modules; correct?               10:08
 8     A  I do.                                           10:07
 9     Q  Okay.  So as a person of ordinary skill in      10:07
10  the art in the field of JEDEC memory modules, the rank 10:07
11  has always meant, in the past and in the present, as  10:07
12  more than one chip?                                   10:07
13        MR. RUECKHEIM:  Object to the form.             10:07
14        THE WITNESS:  Look, you're asking me to give    10:07
15  an opinion on something that I have not prepared.  I   10:07
16  don't know the whole history of all the JEDEC memory  10:07
17  modules.  Even though I claim that I am an expert in   10:07
18  JEDEC memory modules relevant to these patents, you're 10:07
19  asking me something well beyond what I prepared for.   10:07
20        MR. SHEASBY:  I understand that.               10:07
21     Q  Now answer my question:  As a person of        10:07
22  ordinary skill in the art who purports to be an expert 10:07
23  in JEDEC, plain and ordinary meaning of rank, in the  10:07
24  present and past, has always been more than one chip?  10:07
25        MR. RUECKHEIM:  Object to the form of the       10:08
                                                        Page 45
```

12 (Pages 42 - 45)

1  question.                              10:08
2      THE WITNESS: I -- I can't answer for all the  10:08
3  JEDEC in the past. I just simply cannot do that.    10:08
4      MR. SHEASBY: Q. As far as you understand    10:08
5  it.                                  10:08
6      MR. RUECKHEIM: Same objection.          10:08
7      THE WITNESS: Well, let me -- you know, let   10:08
8  me give you an example out of my book. At the last  10:08
9  definition, I showed what are banks, which at that   10:08
10  time could be called ranks, and they were 8-bits wide.  10:08
11  Okay. So I didn't have 72-bit-wide memory. I had   10:08
12  8-bit-wide bytes. Okay.                  10:08
13      So, you know, things change. Along the line,  10:08
14  between then in 1980 and whenever JEDEC started doing  10:08
15  their standards, there could have been memory modules  10:08
16  with 16-bits wide or 32-bits wide.            10:08
17      MR. SHEASBY: Yep.                 10:08
18      THE WITNESS: Okay. And now we're talking   10:08
19  about would those memory modules have multiple chips  10:08
20  in a rank? You know, I have to look that up. I      10:09
21  could, but I have not done that.             10:09
22      MR. SHEASBY: Fair point. Let me ask it this  10:09
23  way: Once JEDEC was created and they began to specify  10:09
24  memory -- DDR memory devices, the width was either 64  10:09
25  or 72; correct?                       10:09

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1      Q  What does 64- and 72-bits wide mean -- mean   10:11
2  to you in the context of DDR?               10:11
3      A  Memory rank.                     10:11
4      Q  In the constant of -- in the context of JEDEC  10:11
5  DDR -- -- POSAs understand that memory rank is defined  10:11
6  in advance as either 64 or 72 bits. There's no other  10:11
7  options?                            10:11
8      MR. RUECKHEIM: Object to the form.         10:11
9      THE WITNESS: I have not explored that       10:11
10  question for DDR and DDR2. I believe if I explored it  10:11
11  I would find that it's probably the case. So        10:11
12  provisionally, I would say, yeah, it could be the     10:11
13  case. I have not -- I've not confirmed that.        10:11
14      MR. SHEASBY: Q. In terms of building JEDEC   10:11
15  DDR devices, has there been an innate -- instance when  10:11
16  you're aware of where people have altered the rank    10:11
17  of -- the width of the -- the bit width of the ranks   10:11
18  from either 64 or 72?                    10:12
19      A  I have.                        10:12
20      Q  For JEDEC-compliant memory devices?       10:12
21      A  Yes.                          10:12
22      Q  When was that?                   10:12
23      A  I plug in a 64-bit module. I take it out, I   10:12
24  plug in a 72-bit module.                   10:12
25      Q  Okay. You understand that on the module    10:12

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1      A  In the DDR and the DDR2 standards, the widths  10:09
2  are 64 and 72, that is correct.             10:09
3      Q  Okay. And for widths of 64 and 72, that --    10:09
4  in the context of JEDEC DDR, a rank is always more    10:09
5  than one chip?                        10:09
6      MR. RUECKHEIM: Object to the form.         10:09
7      THE WITNESS: Again, in the past it has been   10:09
8  more than one chip and --                  10:09
9      MR. SHEASBY: Okay. Great. Thank you.      10:09
10      Q  Now, JEDEC doesn't allow the -- the width of  10:09
11  memory devices to dynamically change; correct? If    10:10
12  you're dealing with JEDEC -- in the context of JEDEC,  10:10
13  the width of the memory device is going to be defined.  10:10
14  People can't just randomly change it. It's either    10:10
15  going to be 64 or 72.                    10:10
16      A  We're -- you know, your question makes no    10:10
17  sense to me.                         10:10
18      Q  Okay. Let me try it this way: When people   10:10
19  are designing memory devices in the context in the    10:10
20  background of -- of JEDEC, they understand that the   10:10
21  way -- the width is either going to be 64 or 72,      10:10
22  depending on the DDR specification?           10:10
23      A  The width of what?                  10:10
24      Q  Of the -- the DDR memory devices.        10:10
25      A  Doesn't make any sense.              10:11

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1  level, it's either 64 or 72; correct?           10:12
2      A  And we're talking -- for the DDR, DDR2, it's   10:12
3  my understanding, but I have not confirmed it, that    10:12
4  they're either 64 or 72.                   10:12
5      Q  Okay. How about for DDR3, DDR4, and DDR5?    10:12
6      A  I have not been asked to opine on those. I    10:12
7  have not studied those.                   10:12
8      Q  Okay. Let's go to the '215 patent.         10:12
9      A  Okay. Let's pull it.                 10:13
10      Okay. I have it up.                   10:13
11      Q  And I'm -- why don't you go ahead and read   10:13
12  column 3, lines 25 to 43, to yourself.          10:13
13      A  Okay. I have read that.              10:13
14      Q  The -- one of the techniques that's described  10:14
15  in the 2Y -- '215 patent is the creating -- creating a  10:15
16  buffer that can control one integrated circuit on the  10:15
17  rank; correct?                        10:15
18      MR. RUECKHEIM: Object to the form.         10:15
19      THE WITNESS: Can you show me that?        10:15
20      MR. SHEASBY: Q. Well, that's -- so -- well,   10:15
21  that's what I'm asking you. I just had you read a     10:15
22  passage, and I'm asking whether that passage is      10:15
23  describing a technique in which the -- you can create  10:15
24  a circuit that can control only one integrated circuit  10:15
25  on the rank, can buffer only one integrated circuit on  10:15

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13 (Pages 46 - 49)

1 the rank?                                    10:15
2    MR. RUECKHEIM:  Same objection.          10:15
3    THE WITNESS:  Your use of the word "buffer"   10:15
4 in your question, can you repeat your question.   10:16
5    MR. SHEASBY:  Sure.  I'm saying -- I will.   10:16
6    Q  So this passage in the specification is   10:16
7 defining a design in which you can have a buffer   10:16
8 circuit that is buffering only one of the integrated   10:16
9 circuits on the rank?                        10:16
10    A  That's not what's said here.         10:16
11    Q  What's being said here?              10:16
12    A  You can buffer the --                10:16
13    MR. RUECKHEIM:  Object to the form.    10:16
14    THE WITNESS:  -- I'm looking at lines 28 and   10:16
15 below.                                      10:16
16    (As read):                            10:16
17    "The register is configured to receive and   10:16
18 buffer the first command and address signals."   10:16
19    And I'm looking -- I don't see any other use   10:16
20 of the word "buffer" in that.  Is that your -- your   10:17
21 question did not indicate what the context the buffer   10:17
22 was when you first asked it.  And later it just -- it   10:17
23 lost all the context.  So I don't know how you mean   10:17
24 they have buffer.                          10:17
25    MR. SHEASBY:  Q.  What is this passage   10:17
                                        Page 50

1 describing, column 3, lines 25 through 43?   10:17
2    A  At a very high level, it describes sending a   10:17
3 first and a second memory command to a memory module.   10:17
4 And, again, at a very high level, it says that the   10:17
5 first memory command receives data or sends data to   10:17
6 one of the ranks and not the other.  And the second   10:17
7 command sends or receives data from the second rank,   10:17
8 but not the other.                         10:17
9    Q  And this contradicts what you said previously   10:18
10 because in this design the rank need only include one   10:18
11 integrated circuit; correct?               10:18
12    A  I didn't contradict anything.  I'm just   10:18
13 reading from this patent.                   10:18
14    Q  Sir, in this design, there only needs to be   10:18
15 one memory-integrated circuit in each rank; correct?   10:19
16    MR. RUECKHEIM:  Object to the form.    10:19
17    THE WITNESS:  In this particular patent, it   10:19
18 says that a rank has at least one, and I believe the   10:19
19 interpretation of that for -- in litigation would be   10:19
20 one would suffice.  That's what it says.  And I --   10:19
21 whether this -- whether it contradicts anything I said   10:19
22 earlier or not is not relevant, because I didn't say   10:19
23 this.  This is what the patent says.         10:19
24    MR. SHEASBY:  Okay.  Let's go to column 37.   10:19
25    Q  Did you look at the claims?          10:19
                                        Page 51

1    A  I did.                             10:19
2    Q  By the way, a memory-integrated circuit is   10:20
3 broader and encompasses more than JEDEC or DDR;   10:20
4 correct?                                    10:20
5    A  I'm sorry.  I don't know what you mean by   10:20
6 "encompasses more than."  What is meant by -- this   10:20
7 is -- I can't understand your question.      10:20
8    Q  Okay.  So you understand -- you know what   10:20
9 memory devices are, DDR memory devices; correct?   10:20
10    A  I do.                              10:20
11    Q  DDR memory devices are devices -- DDR is   10:20
12 defined by JEDEC?                          10:20
13    A  They're --                         10:20
14    MR. RUECKHEIM:  Objection.             10:20
15    THE WITNESS:  -- defined by JEDEC, okay.   10:20
16    Are you asking specifically about DDR devices   10:20
17 defined by JEDEC, or are you defining something more   10:20
18 broadly than that?                         10:20
19    MR. SHEASBY:  Q.  JEDEC defines DDR memory   10:20
20 devices; correct?                          10:20
21    A  That is correct.                    10:20
22    Q  Okay.  And -- but memory-integrated circuits   10:20
23 is broader than just memory devices or DDR memory   10:20
24 devices; correct?                          10:20
25    A  Well, you have two questions in there, and if   10:21
                                        Page 52

1 you want to break them apart, that's fine.  But that's   10:21
2 a compound question.  I'll try to answer each   10:21
3 individually, so why don't you try to ask again.   10:21
4    Q  Memory devices/DDR memory devices are defined   10:21
5 by JEDEC?                                   10:21
6    A  Again --                           10:21
7    MR. RUECKHEIM:  Object to form.         10:21
8    THE WITNESS:  Again, that's compound.   10:21
9 take -- one side is flash and the other side is flash,   10:21
10 and I can answer that.                      10:21
11    MR. SHEASBY:  Q.  DDR memory devices is   10:21
12 defined by JEDEC?                          10:21
13    A  Yes.                              10:21
14    Q  Memory integrated circuits is a broader term   10:21
15 than DDR memory devices?                    10:21
16    A  Yes, because some memory-integrated circuits   10:21
17 are memory devices that are not defined by a JEDEC   10:22
18 standard.  That's correct.                  10:22
19    Q  In other words, there are some            10:22
20 memory-integrated circuits that are not DDR memory   10:22
21 devices?                                    10:22
22    A  That is correct, there are some         10:22
23 memory-integrated circuits that are not JEDEC DDR   10:22
24 devices.                                    10:22
25    Q  Okay.  And now let's go on and look at   10:22
                                        Page 53

                          14 (Pages 50 - 53)

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```
 1  Claim 1 of the patent of the '215.            10:22
 2     A   Okay.                                  10:22
 3     Q   If you look at Claim 1 of the patent in    10:22
 4  the '215, you'll see -- go ahead and read the claim to  10:22
 5  yourself.  It will make it easier and faster.     10:22
 6     A   Okay.                                  10:24
 7     Q   This is talking about a buffer coupled      10:24
 8  between the -- at least one first memory-integrated   10:24
 9  circuit in the memory bus in between at least one     10:24
10  second memory-integrated circuit in the memory bus; do  10:24
11  you see that?                                 10:24
12     A   I do.                                 10:24
13     Q   So this doesn't limit the number of buffers   10:24
14  that can exist; correct?                       10:24
15     A   So there's some legal things that I'm not    10:24
16  familiar with, okay.                          10:25
17        I look -- it says "at least one first      10:25
18  memory-integrated circuit," and I understand there's a  10:25
19  legal position that "at least one" means one or more.  10:25
20  When it says "a buffer," and it doesn't say "at least  10:25
21  one buffer," I don't know legally if that means you    10:25
22  can have two or more or one.  I would have to rely on  10:25
23  counsel on that.                             10:25
24     Q   What does "a" mean, in your understanding, in  10:25
25  patent law?                                  10:25
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 1     A   In patent law, I'm not going to answer      10:25
 2  because I'm not a patent lawyer.               10:25
 3     Q   Okay.  In -- in sort of understanding of a    10:25
 4  POSITA, "a" means one or more; correct?          10:25
 5     A   It -- it -- in ordinary language, "a" means  10:25
 6  one or more, yes.  So my -- my final answer, I thought  10:26
 7  you were asking me something that requires a legal    10:26
 8  opinion, and I'm not qualified for that.          10:26
 9     Q   No, I was asking a technical standpoint.    10:26
10  From a technical standpoint, this would allow for each  10:26
11  memory-integrated circuit and the rank to have its own  10:26
12  buffer?                                       10:26
13        MR. RUECKHEIM:  Object to the form.       10:26
14        THE WITNESS:  Well, there is also an       10:26
15  ambiguity when you say "buffer."  Because a buffer can  10:26
16  comprise many different components, each of which is a  10:26
17  buffer.  So that ambiguity is one of the things I'm    10:26
18  considering.  I mean, I might have eight chips forming  10:26
19  a buffer and I will say all eight chips, that's a     10:26
20  buffer.                                       10:26
21        So it -- because of that ambiguity, I'm not   10:26
22  just sure how to answer your question.           10:26
23        MR. SHEASBY:  Explain that ambiguity to me   10:26
24  again.                                        10:27
25     A   An eight-chip buffer could be referred to as  10:27
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```
 1  a buffer, in the singular, even though it comprises    10:27
 2  eight chips.  And each chip could be described as a    10:27
 3  buffer.  Because each -- each chip buffers something.  10:27
 4  That's the ambiguity.                          10:27
 5     Q   Of what -- I understand.                10:27
 6        There could be separate chips that provide   10:27
 7  buffering functionality to each of the separate      10:27
 8  memory-integrated circuit devices in each ranks      10:27
 9  according to this claim?                       10:27
10        MR. RUECKHEIM:  Object to the form.       10:27
11        THE WITNESS:  Again, you asked a question   10:27
12  that has an ambiguity.  Can you rephrase your       10:27
13  question.                                     10:27
14        MR. SHEASBY:  What's the ambiguity?       10:27
15     A   You said to each chip.  Now, the question was  10:27
16  refers you may have more than one buffer.          10:28
17        Are you saying, then, each chip can have more  10:28
18  than one buffer, or because you have more than one    10:28
19  chip, each chip could have one buffer and in totality  10:28
20  have more than one buffer?  I don't know.         10:28
21     Q   So we have ranks; correct?              10:28
22     A   Yes.                                  10:28
23     Q   Ranks have multiple memory devices in them;  10:28
24  correct?                                      10:28
25     A   That --                               10:28
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 1        MR. RUECKHEIM:  Object to the form.       10:28
 2        THE WITNESS:  -- in -- my understanding is   10:28
 3  that they could have multiple memory devices.       10:28
 4        MR. SHEASBY:  Okay.                    10:28
 5     Q   And in this claim, there can be a dedicated   10:28
 6  buffer for each memory-integrated circuit in the rank?  10:28
 7     A   Well, first of all, the claim applies to one  10:28
 8  memory device, okay.                          10:28
 9     Q   By "memory device," are you meaning        10:28
10  memory-integrated circuit, or do you -- do you mean --  10:28
11     A   Go ahead.                             10:28
12     Q   You said "memory device."  Now that's       10:28
13  ambiguous to me.                             10:29
14     A   Okay.  I should say at least one first      10:29
15  memory-integrated circuit.                     10:29
16     Q   Okay.                                 10:29
17     A   And that you may have only one of those.    10:29
18     Q   You may have only one memory-integrated      10:29
19  circuit?                                      10:29
20     A   That's correct.  And then you need to have at  10:29
21  least one of the second.  So you may have only one     10:29
22  memory -- memory-integrated circuit, and that's       10:29
23  buffered, according to this claim.               10:29
24     Q   Right.  So now I'm asking the -- the -- the   10:29
25  question is:  Does this allow for there to be a       10:29
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15 (Pages 54 - 57)

1  separate buffer for each memory-integrated circuit?    10:29
2      MR. RUECKHEIM:  Object to the form.        10:29
3      THE WITNESS:  It's not specified in the        10:29
4  claim, and so I would have to look elsewhere to see if  10:29
5  such a structure were permitted.            10:29
6      MR. SHEASBY:  Q.  Do you know what the input    10:29
7  control signals are in JEDEC memory modules?        10:29
8      A  I do.                    10:30
9      Q  You do?                    10:30
10     A  I -- I know what the input control signals    10:30
11  are.                        10:30
12     Q  What are they?                10:30
13     A  Okay.  Which -- first of all, the inputs to    10:30
14  the devices, the integrated memory devices, or the    10:30
15  input to the module?                10:30
16     Q  Let's start with integrated to the module.    10:30
17     A  Okay.  We can go to the figure that shows    10:30
18  them.  I think Figure 1 of this patent shows it.    10:30
19     Q  And "this patent," just for the record,    10:30
20  you're referring to the '215; is that correct?    10:30
21     A  That's correct.                10:30
22     Q  Okay.  What are the input signals to the    10:30
23  memory module?                    10:30
24     MR. RUECKHEIM:  Object to the form.        10:30
25     STENOGRAPHIC REPORTER:  I didn't get your    10:30

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1  answer.                    10:30
2      THE WITNESS:  Are you asking for all input    10:30
3  signals or control signals?            10:30
4      MR. SHEASBY:  Q.  Control signals.        10:30
5      A  Those are identified by -- by at least the    10:31
6  lines that say CS with a crosshatch, AD for address,    10:31
7  and the ampersand and control.  So those are the    10:31
8  control signals.  And -- and some people may consider  10:31
9  the DQS signals, the strobes, also as control signals.  10:31
10     Q  So it would be at least the row/column    10:31
11  address, the bank address, and the chip select signal?  10:31
12     A  And the control.                10:31
13     Q  Yes.                    10:31
14     A  And your question is:  Do I consider those    10:31
15  the input control signals?            10:31
16     Q  Yes, sir.                    10:31
17     A  I do.                    10:31
18     Q  And -- and as an alternative to using the    10:32
19  control signals, you can also use packetized    10:32
20  information that is decoded by on-module logic;    10:32
21  correct?                    10:33
22     MR. RUECKHEIM:  Object to the form.        10:33
23     THE WITNESS:  It's not shown this way in the    10:33
24  figure and it's not mentioned in the patent in the --  10:33
25  in the claims.  Are you asking me if I use packetized  10:33

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1  control signals with the practice of the patent?  Is    10:33
2  that your question?                10:33
3      MR. SHEASBY:  That's actually not my        10:33
4  question.                    10:33
5      Q  What I'm saying is, the patent talks about    10:33
6  these control signals; correct?            10:33
7      A  It does.                    10:33
8      Q  And there's an alternative to using control    10:33
9  signals, which is that you can use packetized        10:33
10  information that is then decoded on the -- on the    10:33
11  module?                        10:33
12     A  The context of your question, it says, "you    10:33
13  can use."  Of course I could use.  But there's some    10:33
14  hidden context there.                10:33
15      Is that with respect to practicing the patent  10:33
16  or not practicing the patent?            10:34
17     Q  No, no, I -- it has nothing to do with        10:34
18  practicing the patent -- or practicing the patent.    10:34
19      A POSA just understood -- understands that in  10:34
20  addition to the traditional JEDEC control signals,    10:34
21  there's also an ability to send packetized control    10:34
22  information?                    10:34
23     MR. RUECKHEIM:  Object to the form.        10:34
24     THE WITNESS:  And there's also an ability --    10:34
25  are you asking within the -- any JEDEC standard, or in  10:34

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1  general?                    10:34
2      MR. SHEASBY:  Q.  In general.  In general.    10:34
3      A  In general.                10:34
4      Q  In -- in JEDEC context, there's these four    10:34
5  control signals, they travel in four lines to the    10:34
6  memory module; fair?                10:34
7      A  If -- if you're asking me, as one of skill in  10:34
8  the art, can I build a device in which I send        10:34
9  packetized control signals to a module, the answer is,  10:34
10  yes, I could.                    10:34
11      So if -- if that's the question, the answer    10:34
12  is yes.  But I don't know if there's a context that's  10:34
13  hidden, so I can't be sure of what you mean.        10:35
14     Q  All right.                10:35
15      So the context, this is -- JEDEC doesn't do    10:35
16  that.  JEDEC uses the four control signals traveling    10:35
17  on four wires?                    10:35
18     A  And that's because of the timing in this --    10:35
19  okay.                        10:35
20      In my understanding, the DDR and the DDR2    10:35
21  standards have timing for the control signals.  And    10:35
22  that timing, whatever it is, is -- the control signals  10:35
23  are sent as control.  In some cases, it may take --    10:35
24  take more than one clock to get eight commands across;  10:35
25  okay.                        10:35

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16 (Pages 58 - 61)

1     So I -- is that packetized? I -- packetized     10:35
2   is not defined in the standard, and I'm aware of     10:35
3   instances where it takes more than one clock cycle to     10:35
4   send a command.                                  10:35
5     Q   Right.                                      10:35
6       I guess what I'm saying is, as an alternative     10:35
7   to the JEDEC method of sending the control signals,     10:35
8   there's also -- you could also -- an alternative way     10:36
9   of doing it would be to use packetized information     10:36
10  that is then decoded by the ON-logic.             10:36
11    A   It's my understanding that DDR and DDR2, in     10:36
12  some instances, send commands over more than one clock     10:36
13  cycle and decodes them; and, therefore, it's my     10:36
14  understanding, that's packetized.                 10:36
15    Q   So you -- you think JEDEC uses packetized     10:36
16  control information?                             10:36
17    A   I -- I'm not saying that.  I'm trying to     10:36
18  figure out if -- if what JEDEC does satisfies your     10:36
19  words "packetized."                              10:36
20    Q   Let me ask you this:  You understand that you     10:36
21  can send a signal; right?                        10:36
22    A   Yes.                                        10:36
23    Q   Signal is one clock cycle; correct?          10:36
24    A   A signal is interpreted over one clock cycle,     10:36
25  yes.                                             10:36

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1   Q   And in addition to sending a signal, you can     10:36
2   also send packetized control information; correct?     10:36
3       MR. RUECKHEIM:  Object to the form.          10:36
4       THE WITNESS:  In addition to; but that's not     10:36
5   in addition to.                                  10:37
6       MR. SHEASBY:  All right.                     10:37
7     Q   So if -- if the data that you're transmitting     10:37
8   is over more than one clock cycle, then it ends up     10:37
9   becoming packetized.  It's not just a signal?     10:37
10    A   That's what you say.  But that's okay.  If     10:37
11  that's what you say, I'll accept it.  That's what you     10:37
12  mean by "packetized."                            10:37
13    Q   No, I'm trying to get at your understanding     10:37
14  of "packetized."                                 10:37
15    A   I'm trying to get at yours.                  10:37
16    Q   That's irrelevant.                          10:37
17    A   It is -- it is -- let's agree on this:  It is     10:37
18  the case that DDR/DDR2 sends commands over more than     10:37
19  one cycle and decodes them on the memory module.  That     10:37
20  is the case.                                     10:37
21    Q   Right.                                      10:37
22      And it also has the ability to send a single     10:37
23  signal within one clock cycle?                    10:37
24      MR. RUECKHEIM:  Object to the form.          10:37
25      THE WITNESS:  It does.  It sends a single     10:37

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1   signal within one clock cycle.  In fact, it has better  10:37
2   than that.  It can send two signals in one clock     10:37
3   cycle.                                           10:38
4       MR. SHEASBY:  Q.  So in addition to send --     10:38
5   using -- passing control information over signals, it     10:38
6   can also pass control information packetized?     10:38
7     A   Your word is "packetized."  It can send -- it     10:38
8   can send commands over more than one clock cycle.     10:38
9   That's my testimony.                             10:38
10    Q   And you describe that -- that can be          10:38
11  described as packetized?                         10:38
12    A   No, you described it packetized.  I never --     10:38
13  I'm asking you if it satisfies your definition.     10:38
14    Q   I don't --                                  10:38
15    A   You're calling that packetized.              10:38
16    Q   All right.                                  10:38
17      So what is packetized control and address     10:38
18  information for you?                             10:38
19    A   I'm sorry.  I haven't prepared that for this     10:38
20  deposition.  I don't -- I gather that packetized is     10:38
21  sending something over more than one clock cycle.     10:38
22    Q   Okay.  That's the common understanding of     10:38
23  packetized?                                      10:38
24    A   That is --                                  10:38
25      MR. RUECKHEIM:  Object to the form.           10:38

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1       THE WITNESS:  -- I think that a person of     10:38
2   ordinary skill in the art would say that when     10:38
3   something is packetized it takes more than one cycle     10:39
4   to send that information, yes.                    10:39
5       MR. SHEASBY:  Okay.                          10:39
6     Q   JEDEC styles memory module systems feature     10:39
7   for distinct buses; is that correct?             10:39
8       MR. RUECKHEIM:  Object to the form.          10:39
9       THE WITNESS:  Well, if you don't mind telling     10:39
10  the four distinct bus.  I want to know what's in your     10:40
11  mind in that question.  I can't answer it as asked.     10:40
12      MR. SHEASBY:  Sure.                          10:40
13    Q   For the SDRAMs in -- okay.  We'll do it in     10:40
14  pieces.                                          10:40
15      You know what DRAM circuits are; right?       10:40
16  They're these monolithic DRAM chips.             10:40
17    A   Such as in Figure 1, the Device 32.          10:40
18    Q   So you accept that as what a DRAM circuit is;     10:40
19  correct?                                         10:40
20    A   I accept it.  I -- I will -- Device 32 will     10:40
21  be a DRAM -- a DRAM circuit, yes.                 10:40
22    Q   Okay.  So we have DRAM circuits which are     10:40
23  monolithic chips containing DRAM cells; correct?     10:40
24    A   DRAM cells, you said.                        10:40
25    Q   DRAM cells, yes.                            10:40

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17 (Pages 62 - 65)

1    A   So 30 is a DRAM cell?                10:41
2    Q   No, no. I'm just trying to get some -- some   10:41
3  common -- what's a DRAM circuit?              10:41
4    A   A DRAM circuit, as an integrated chip, would   10:41
5  be an integrated chip that contains DRAM memory cells. 10:41
6    Q   A monolithic DRAM memory cell?           10:41
7       MR. RUECKHEIM: Object to the form.       10:41
8       MR. SHEASBY: Q. Here's what I'm asking: Do   10:41
9  you consider a chip that has embedded DRAM on it to be 10:41
10  a DRAM circuit?                          10:41
11   A   It depends.                         10:41
12   Q   Tell me why.                         10:41
13   A   I can build a FPGA that mimics a DRAM. After   10:41
14  I program it to mimic the DRAM, I would consider it a   10:41
15  DRAM circuit.                            10:41
16   Q   What about a processor that has embedded DRAM  10:41
17  on it?                                  10:41
18   A   Oh, I understand. It could have more than      10:42
19  just DRAM and you would have a complex chip of some   10:42
20  sort. I understand that. That could happen.        10:42
21   Q   So if you have more than just DRAM and DRAM    10:42
22  circuitry on it, it no longer -- you understand that's 10:42
23  not a DRAM circuit?                        10:42
24   A   I just can't --                      10:42
25       MR. RUECKHEIM: Object to the form.       10:42
                                              Page 66

1       THE WITNESS: -- presume that I would      10:42
2  understand it is, that is --                   10:42
3       STENOGRAPHIC REPORTER: I'm sorry. I'm     10:42
4  sorry. If you can please start that over. The      10:42
5  objection. Covered you.                     10:42
6       MR. RUECKHEIM: Object to the form.       10:42
7       MR. SHEASBY: Go ahead.                 10:42
8       THE WITNESS: I gave an example just a moment   10:42
9  ago of an FPGA that have more than just DRAM on it,   10:42
10  program to mimic a DRAM. And at that point, I call it 10:42
11  a DRAM circuit. And it fit your definition of things   10:42
12  that I would not call a DRAM circuit. So I think I    10:42
13  would still call that a DRAM circuit. So I -- I would  10:42
14  answer your question no.                     10:42
15       MR. SHEASBY: Q. A circuit that is complex   10:42
16  functionality beyond that that is just used to store  10:43
17  information in DRAM memory cells is not a DRAM        10:43
18  circuit?                                10:43
19       MR. RUECKHEIM: Object to the form.       10:43
20       THE WITNESS: If that complex functionality  10:43
21  is used just for programming the FPGA and then it's no 10:43
22  longer used, you still have a DRAM circuit.        10:43
23       So I know what you're trying to get at, but  10:43
24  your questions don't allow me to say yes.          10:43
25       MR. SHEASBY: I understand. I'll work on it 10:43
                                              Page 67

1  and I appreciate you -- you keeping me precise.      10:43
2    Q   Chips that have functionality on them that is  10:43
3  other than the functionality that is used to store   10:43
4  memory, store information in memory is something     10:43
5  different than a DRAM circuit?                 10:43
6       MR. RUECKHEIM: Object to the form.       10:43
7       THE WITNESS: That still fits a FPGA that --   10:43
8  that is programmed to be a DRAM. So I can't answer    10:44
9  "yes" to your -- your question.                 10:44
10       MR. SHEASBY: Okay.                   10:44
11   Q   So chips that do have information -- have      10:44
12  structure on them other than structure that's used to 10:44
13  program them to act like a DRAM, or to actually have  10:44
14  DRAM memory cells on them, those are not DRAM        10:44
15  circuits?                               10:44
16       MR. RUECKHEIM: Same objection.          10:44
17       THE WITNESS: Vague as to what you mean by    10:44
18  the other circuitry.                        10:44
19       If you sharpen that up, I'll be able to      10:44
20  answer the question. I can't answer it with --       10:44
21  without knowing what's going on in these chips.       10:44
22       MR. SHEASBY: Q. If you have chips that do    10:44
23  things like have -- do you know -- you know the        10:44
24  complex structure that's used in -- in -- to connect  10:45
25  chips together using TSV; correct?              10:45
                                              Page 68

1    A   What kind of chips?                   10:45
2       MR. RUECKHEIM: Object to form.          10:45
3       MR. SHEASBY: Q. That -- chips connecting    10:45
4  chips, stacked chips, together using TSVs,          10:45
5  through-silicon vias.                       10:45
6       Are you familiar with the technology?       10:45
7    A   Your acronym is vague. It's either FPG,      10:45
8  or -- can you spell out your acronym so I know exactly 10:45
9  what acronym you're using?                   10:45
10   Q   Through-silicon via.                   10:45
11   A   Ah, TSVs. Yes, I'm familiar with that, yes.   10:45
12   Q   And you understand that to be able to        10:45
13  transfer information between chips in TSVs it takes   10:45
14  significant functionality on the chip?            10:45
15   A   I don't know how to answer your question.     10:45
16  What chip are you talking about has -- what         10:46
17  functionality? I don't understand what you're -- what 10:46
18  your question is.                         10:46
19   Q   All right. Let me get at it this way, this   10:46
20  may be easier, SDRAMs have memory buses, data address 10:46
21  control, and chip select buses; correct?          10:46
22   A   That's correct.                      10:46
23   Q   And when -- when a logic element receives the  10:46
24  four control signals we've talked about from the     10:46
25  memory system, not all four of those signals may be   10:47
                                              Page 69

18 (Pages 66 - 69)

| | |
|---|---|
| 1  used in any one instance; is that correct?          10:47 | 1  individual device?                              10:49 |
| 2     A  First of all, we need to identify the control  10:47 | 2     A  Okay.  Now, when you say they are not used,    10:49 |
| 3  signals again just so I know what question I'm asking.  10:47 | 3  and you're saying they're not used on the module or    10:49 |
| 4  But there's more than four control systems going to    10:47 | 4  not used on the device?  I have to understand your --  10:49 |
| 5  the chip so I'm confused already.             10:47 | 5     Q  Not used on the device.              10:49 |
| 6     Q  I'm not talking about the chip, I'm talking    10:47 | 6     A  On the device.  So it may be the case --    10:49 |
| 7  about the memory module.                  10:47 | 7  these, we're talking about bank selects; right?     10:49 |
| 8     A  To the memory module, there's more than four  10:47 | 8     Q  Yes, sir.                        10:49 |
| 9  control signals.                        10:47 | 9     A  It may be the case that the bank selects were  10:50 |
| 10    Q  All right.  You don't need to use all of the    10:47 | 10  not passed on to devices without modification, but    10:50 |
| 11  memory -- all the control signals that are sent to the  10:47 | 11  those bank selects will be used on the module and    10:50 |
| 12  memory module for any one act; correct?         10:47 | 12  cause some things to change or cause some -- some    10:50 |
| 13    A  Why don't you specify the signals that you    10:47 | 13  information to be sent to the memory devices.      10:50 |
| 14  want to use and the signals that you don't want to use  10:47 | 14    Q  But they may not be sent to the memory    10:50 |
| 15  so I know to answer -- what question I'm answering.    10:47 | 15  devices; correct?                     10:50 |
| 16    Q  So what are all the control signals that are    10:47 | 16     Here's -- let me give you an example, and    10:50 |
| 17  sent to the memory module?                10:47 | 17  this may be the starkest.  You receive bank address    10:50 |
| 18    A  To that, we would bring up --          10:47 | 18  signals and chip address -- chip select signals from    10:50 |
| 19     MR. RUECKHEIM:  Object to form.         10:47 | 19  the -- from the memory controller?            10:50 |
| 20     THE WITNESS:  -- a DDR standard.  I can show   10:47 | 20    A  Yes.                          10:50 |
| 21  you that.  Do you have a DDR standard for a memory    10:47 | 21    Q  You don't use the bank address signal to    10:50 |
| 22  module?                          10:48 | 22  generate the chip select signal that goes on -- that  10:50 |
| 23     MR. SHEASBY:  Q.  Give me the ones you know.  10:48 | 23  goes to the chip?                     10:50 |
| 24    A  The ones I have?                 10:48 | 24    A  I'm not aware of that ever happening.      10:50 |
| 25    Q  The ones we've talked about previously.    10:48 | 25    Q  Okay.                        10:51 |
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| | |
|---|---|
| 1     A  DDR --                       10:48 | 1     THE VIDEOGRAPHER:  Counsel Sheasby, this is    10:51 |
| 2     Q  We talked about --                10:48 | 2  the videographer.  May we take a media break in the    10:51 |
| 3     A  DDR, let's see.  DDR and DDR2; the DIMM      10:48 | 3  next five minutes?                     10:51 |
| 4  standards, we looked at that.              10:48 | 4     MR. SHEASBY:  Sure.  Let's do it now.      10:51 |
| 5     Q  Maybe this is an easier way of doing it.     10:48 | 5     THE VIDEOGRAPHER:  Thank you.           10:51 |
| 6  When looking at the patent, we've identified control   10:48 | 6     Is that okay, Counsel Rueckheim?        10:51 |
| 7  signals that go from the memory module, go from the    10:48 | 7     MR. RUECKHEIM:  Yes.                10:51 |
| 8  system to the memory module, or the controller to the  10:48 | 8     THE VIDEOGRAPHER:  We're going off the      10:51 |
| 9  memory module; correct?                 10:48 | 9  record.  This is the end of Media Unit 2.  The time is  10:51 |
| 10    A  Okay.                        10:48 | 10  10:51 a.m.                         10:51 |
| 11    Q  And those can involve chip select as well as   10:48 | 11    (Recess taken.)                   10:51 |
| 12  bank select; is that correct?              10:48 | 12     THE VIDEOGRAPHER:  We're back on the record.   11:00 |
| 13    A  That is correct.                 10:48 | 13  This is the beginning of Media Unit 3.  The time is    11:00 |
| 14    Q  And even though all those four signals are    10:48 | 14  11:00 a.m.                         11:00 |
| 15  sent, for any one signal that is passed on to a device  10:48 | 15     MR. SHEASBY:  Q.  What is CAS?          11:00 |
| 16  you may not use -- a memory device, you may not use    10:48 | 16    A  CAS is the name for one of the signals that   11:00 |
| 17  all four of those signals to control the memory      10:48 | 17  control a chip.  It is -- the name is column address   11:00 |
| 18  device?                          10:48 | 18  strobe, and it -- it has a historical significance.    11:01 |
| 19    A  What do you mean by "may not use"?       10:49 | 19  It's a little less significant today.  They left the   11:01 |
| 20    Q  For example, you may not use the bank       10:49 | 20  name alone as they changed the function.        11:01 |
| 21  address.                          10:49 | 21    Q  What is the current function?          11:01 |
| 22    A  The bank add- -- bits that go in, do       10:49 | 22    A  It's used to -- as part of the protocol for   11:01 |
| 23  something.  They control logic.  I believe they are    10:49 | 23  selecting chips and sending data.            11:01 |
| 24  used.                             10:49 | 24    Q  And what is latency in the context of CAS?   11:01 |
| 25    Q  Even if they may not be passed on to the     10:49 | 25    A  I think the easiest thing to do to see, a    11:01 |
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19 (Pages 70 - 73)

1  timing diagram showing that latency, and I wonder    11:01
2  if -- I don't think the '215 and '417 patent have such  11:01
3  a timing diagram. I'd like to have something in front  11:01
4  of me. It's easier to explain. Do you happen to have  11:01
5  a --                    11:01
6    Q  The '912 may have a timing diagram in it.    11:01
7    A  That would be excellent. I know the '912.    11:02
8  Let's bring that up.                11:02
9    Q  I think Figure 5 has a timing diagram in it.    11:02
10    A  Okay. I have the '912 on my screen.    11:02
11    Q  And there's a number of timing diagrams in    11:02
12  Figure 4 and Figure 5. Let me know if those help you.  11:02
13  My guess is the Figure 5 timing diagram is the one    11:02
14  that is going to help.                11:02
15    A  Okay. These -- these show the latency, but    11:02
16  not the CAS latency. So I -- let me do -- let me    11:03
17  pretend that there's a CAS signal and I can talk about  11:03
18  CAS -- CAS latency, and I'm going to work with    11:03
19  Figure 4.                11:03
20    Q  Go for it.                11:03
21    A  Okay. There's a command line that says "Read  11:03
22  A" that's a command to do a read.        11:03
23      Let us suppose that the command has been    11:03
24  issued earlier and what we see where it says "Read    11:03
25  A" is a CAS single, which is a single to the chips    11:03

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1  that now is the time just to go through your    11:03
2  machinations to produce data.        11:03
3      You see where it says "Data A"?        11:03
4    Q  Yes.                11:04
5    A  Okay. Data A has now been produced at the    11:04
6  output of that chip as a result of the CAS single, the  11:04
7  pseudo-CAS single that I have inserted in Read A. And  11:04
8  the time between the Read A and the appearance of the  11:04
9  data is called the CAS latency.        11:04
10      Basically, that's the time that it takes the    11:04
11  chip to produce the data once it has been found that  11:04
12  it has to produce the data. Okay.        11:04
13      I -- I have better pictures of that        11:04
14  elsewhere.                11:04
15    Q  Yeah, I should have brought in a better    11:04
16  picture as well, it's true.        11:04
17      The CAS latency can apply to both read and    11:04
18  write; is that correct?            11:04
19    A  It -- it's a related to the write. CAS    11:05
20  latency, they're usually in the DDR specifications.    11:05
21  They speak of a read CAS latency and a write CAS    11:05
22  latency. And if we're going to do that, let's bring    11:05
23  up those standards so we can see what they're talking  11:05
24  about.                11:05
25    Q  Let's actually go to column 22 of the '215    11:05

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1  patent.                    11:05
2    A  Okay. I'm in column 22.            11:05
3    Q  Actually, I think column 20. I think I got    11:05
4  it wrong. Let me find it again.            11:05
5    A  I'm in column 20.            11:05
6    Q  Let me do a word search.            11:05
7      Yeah, it's column 20. If you read through    11:06
8  column 20, lines 21 through 49, or 48.        11:06
9    A  That's the paragraph that starts "in certain    11:06
10  embodiments, the Circuit 40 comprises"; is that    11:06
11  correct?                11:06
12    Q  Yes.                11:06
13    A  Okay. And I should read that to myself?    11:06
14    Q  Yes.                11:07
15    A  Okay.                11:07
16    Q  This passage is indicating that CAS latency    11:07
17  can relate to both read and write data transfers?    11:08
18    A  That's correct.                11:08
19      MR. RUECKHEIM:  Object to the form.        11:08
20      MR. SHEASBY:  Okay.            11:08
21    Q  Now, let's go to Figure 6A of the '215    11:08
22  patent. And I believe that's also -- well, yeah,    11:08
23  let's go to 6A.                11:08
24    A  I'm at Figure 6A.            11:08
25    Q  And let's also look at column 11, lines 38    11:08

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1  through 57.                11:08
2    A  Okay. Just a moment. That's the paragraph    11:09
3  that begins "in certain embodiment when the second    11:09
4  read command..." et cetera?            11:09
5    Q  I know it's the paragraph above that, I    11:09
6  think. Wait. Actually, why don't you go ahead and    11:09
7  read column 38, through -- column 11, lines 38,    11:09
8  through column 12, lines 4?            11:09
9    A  All right. Column 11. And 38 begins "Due to  11:09
10  their synchronous nature, DDR SDRAM..." that's where  11:10
11  you start?                11:10
12    Q  Yes, sir.                11:10
13    A  And how far do I read?            11:10
14    Q  To column 12, line 2.            11:10
15    A  Okay. Okay.            11:10
16    Q  Give me one second.            11:11
17      What's a strobe suggest signal?        11:11
18    A  Please give me context because there's many    11:12
19  different contexts.            11:12
20    Q  What's a data strobe signal?        11:12
21    A  A data strobe signal. Okay. Let's go to the  11:12
22  figure you have. Figure, is it 6 that you're looking  11:12
23  at?                11:12
24    Q  Sure.                11:12
25    A  Okay. One moment.            11:12

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20 (Pages 74 - 77)

1    Q  I think I was looking at Figure 7, but you    11:13
2  can use Figure 6 if you prefer.    11:13
3    A  I'm trying to rotate it on my screen. Just a    11:13
4  moment. Got it. Figure 6 works better for me at the    11:13
5  moment.    11:13
6    Q  Sure.    11:13
7    A  This is fairly simplified. I'm looking at    11:13
8  Figure 6A. There's a clock that goes up and down, up    11:13
9  and down. A cycle on the clock is an up period    11:13
10  followed by a down period, and the length of a cycle    11:13
11  is indicated by the vertical dashed lines.    11:13
12      You see the signal called DQS. That's a    11:13
13  strobe. The strobe provides the timing for reading    11:13
14  the data and a double data rate. So the preamble on a  11:14
15  burst of strobes starts with the strobe going down.    11:14
16  Otherwise, you see it's at an intermediate point?    11:14
17  Okay. So the signal that you're going to start a    11:14
18  burst is the drop that occurs in the third cycle in    11:14
19  Figure 6A.    11:14
20      The data is timed to start appearing after    11:14
21  the strobe. Now, this time at which it appears is a    11:14
22  function of the latency -- of the CAS latency of the    11:14
23  device.    11:14
24      So earlier, when a read command comes in and    11:14
25  then the CAS latency appears to the device, it starts    11:14

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1  counting clock cycles, and it expects the data to    11:15
2  appear, at its input pin, the amount of that read    11:15
3  latency.    11:15
4      Write commands work similarly, but not quite    11:15
5  the same. If that write command were where the first  11:15
6  Read A is -- sorry -- the write command issued earlier  11:15
7  and then the read command were the CAS, the CAS    11:15
8  control command for the right, then the -- again, the  11:15
9  device would start counting cycles. And it would    11:15
10  expect the data from the computer to appear on its    11:15
11  input a certain number of cycles later. And that    11:15
12  would be the write CAS latency. It need not be the    11:16
13  same as the read CAS latency.    11:16
14      Well, given that the data will either be    11:16
15  generated from the chip on a read or generated from    11:16
16  the computer and sent to the chip on the write, we now  11:16
17  have DQ bits appearing on a bus.    11:16
18      Okay. On the write, that's -- we're going to  11:16
19  pretend we have a write, the chip will look at the    11:16
20  strobe, the DQS signals, and it will sample the data    11:16
21  on the falling edge of a DQS and the rising edge of a  11:16
22  DQS.    11:16
23      So you see in the fourth clock cycle, the    11:16
24  strobe falls and then rises and the two bits from the  11:16
25  computer are written into the memory, into the DDR    11:17

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1  memory device. And that continues through the length  11:17
2  of the burst. We get two for the price of one because  11:17
3  we have an up and a down. That's why it's called    11:17
4  double data rate.    11:17
5      Reads work a little differently. When you    11:17
6  wait the required read CAS latency, the chip produces  11:17
7  the bits on its output. And with that, it also    11:17
8  produces the strobe signals. They're generated at the  11:17
9  chip. And they go out to the memory.    11:17
10      You could, in theory, have one strobe --    11:17
11  strobe for each bit, but that's not the usual case.    11:17
12      Normally it's one strobe for every eight or    11:18
13  one strobe for every four, and the standards can    11:18
14  change.    11:18
15      And the reason for the strobe is that path    11:18
16  lengths differ depending on where you are in the 64-    11:18
17  or 72-bit chain.    11:18
18      So instead of having one clock that could be    11:18
19  received by all devices at different times, you send    11:18
20  the clock that goes along the same length pathway as    11:18
21  the bits that it's controlling, and that's why we have  11:18
22  strobes.    11:18
23      So in this case, for the read command, those    11:18
24  strobes follow the bits through the memory module out  11:18
25  to the computer, and the computer receives the bits at  11:18

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1  the time it expects it and writes those bits into    11:18
2  memory according to the strobe's falling edge, rising  11:18
3  edge. So that's -- that's latency and that's strobes.  11:18
4      How's that?    11:18
5    Q  Sure. That's fine.    11:19
6      And you see what I've drawn here in this red    11:19
7  box?    11:19
8    A  I -- I have to -- I'm looking at my own copy.    11:19
9  So let me know -- see what we're looking at. Is it on  11:19
10  the screen?    11:19
11    Q  Yes.    11:19
12    A  I have to bring that up. Okay. I got it. I    11:19
13  see a red box.    11:19
14    Q  This is a series of data strobes; is that    11:19
15  correct?    11:19
16    A  That's correct.    11:19
17    Q  And it leads to a gapless read of data; is    11:19
18  that correct?    11:19
19    A  That -- I'd have to look at what the text of    11:19
20  the patent says. I believe that's a gap -- gapless    11:19
21  read, but I need to confirm that. I see no gap.    11:19
22    Q  Okay. Go ahead and confirm that.    11:19
23      But by -- by "this" I -- I -- the red box    11:19
24  is -- that I've drawn here is a continuous series of    11:19
25  data strobes.    11:20

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21 (Pages 78 - 81)

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```
 1    A  It is.                         11:20
 2    Q  Okay.                          11:20
 3    A  It is.                         11:20
 4    Q  And I'll mark this as the next exhibit. I'll   11:20
 5  mark this as Exhibit 12 now.              11:20
 6      (Document remotely marked Exhibit 12        11:20
 7       for identification.)               11:20
 8      THE WITNESS:  Okay.              11:20
 9      MR. SHEASBY:  Q.  And I'll let you go ahead,   11:20
10  and you were going to review.             11:20
11    A  6A.  I have to shrink the screen.  I'm going   11:20
12  to be very careful.  I'm having difficulty shrinking   11:20
13  my screen so I can read the 6A.  If you can bring the   11:21
14  description 6A on your screen, that would be easier   11:21
15  for me.                          11:21
16    Q  Give me one second.  I'm just adding this     11:21
17  exhibit and then I will do that next.          11:21
18    A  Okay.                        11:21
19    Q  Okay.  You wanted me to show you on my      11:21
20  screen --                         11:21
21    A  Oh, I can do it on mine.  I learned how to do   11:21
22  it.                            11:21
23    Q  I'll tell you what, I will put up Figure 6 --   11:21
24    A  Okay.                        11:21
25    Q  -- on my screen, and then you can have the    11:21
```

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```
 1  break.  Well, let's go a couple more minutes and then   11:24
 2  we can take a break.                   11:24
 3      If you go down to -- you said you read       11:24
 4  the '912 patent; is that correct?  You said you're    11:24
 5  familiar with it?                     11:24
 6    A  I'm familiar with which patents now?        11:24
 7    Q  The '912 patent.                  11:24
 8    A  The two patents that I'm familiar with that    11:24
 9  I'm testifying on are the '215 and the '417.       11:24
10    Q  I know, but, I mean, you read the '912 patent   11:24
11  as well; correct?                     11:24
12    A  I've not prepared -- I have read it and      11:24
13  looked at it, but I haven't prepared for the      11:24
14  deposition of reading it.                11:24
15    Q  Okay.  So let's go to the '215 and look at    11:24
16  the claims.  And look at Claim 1 of the '215 patent.   11:24
17    A  Okay.  I don't have the whole Claim 1 on my    11:25
18  screen.  Do you want me to do it on mine?  I'll read   11:25
19  it on my screen.                     11:25
20    Q  Let me go ahead and stop sharing, because     11:25
21  that's going to be confusing.              11:25
22    A  Okay.  You want me to read all of Claim 1; is   11:25
23  that correct?                       11:25
24    Q  To yourself.                    11:25
25    A  Okay.                        11:25
```

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```
 1  text on your screen.                   11:22
 2    A  Okay.  I've got the text, and I...         11:22
 3      I see Figure 6A.  I'll read the pertinent      11:22
 4  parts so we understand what I'm looking at.       11:22
 5      (As read):                    11:22
 6      "Figure 6A shows exemplary" -- "an exemplary    11:22
 7  timing diagram of this gapless read burst for a      11:23
 8  back-to-back adjacent read condition from one memory   11:23
 9  device."                         11:23
10      Okay.  All right.  I believe that's my answer   11:23
11  to your question.                    11:23
12    Q  So it's a continuous burst of -- of reads?    11:23
13      MR. RUECKHEIM:  Object to the form.        11:23
14      THE WITNESS:  It's a continuous burst -- let   11:23
15  me think about that.                   11:23
16      I'm only going to agree to what the patent     11:23
17  says.  It says it's a gapless read burst.        11:23
18      MR. SHEASBY:  Okay.              11:23
19    Q  And that gapless read burst is based on a     11:23
20  burst of continuous data strobes that we see in the   11:23
21  red box above; correct?                 11:23
22    A  It's a continuous date -- ah, that's an      11:23
23  interesting question.                  11:23
24    Q  Let me ask it this way -- let me ask it this   11:23
25  way -- actually, you know what, we need to take our   11:24
```

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```
 1    Q  To yourself.                    11:25
 2    A  Okay.                        11:27
 3    Q  So you're looking at -- Claim 1 of the '215    11:27
 4  patent is not limited to DDR memory devices; correct?  11:28
 5      MR. RUECKHEIM:  Object to the form.        11:28
 6      THE WITNESS:  Well, it does not say it's     11:28
 7  limited to DDR memory devices.  So presumably there   11:28
 8  may be memory devices that are not DDR that might    11:28
 9  practice the claims of the patent, claim -- of      11:28
10  Claim 1.                         11:28
11      MR. SHEASBY:  Okay.  Let's take a break.     11:28
12  I'll need 10 or 15 minutes.              11:28
13      THE WITNESS:  Okay.  Thank you.          11:28
14      THE VIDEOGRAPHER:  We're going off the      11:28
15  record.  This is the end of Media Unit 3.  The time is   11:28
16  11:28 a.m.                        11:28
17      (Recess taken.)                 11:28
18      THE VIDEOGRAPHER:  We are back on the record.  11:46
19      This is the beginning of Media Unit 4.  The    11:46
20  time is 11:46 a.m.                   11:46
21      MR. SHEASBY:  Q.  Dr. Stone, did you have any   11:46
22  discussions with your counsel on any of the breaks?    11:46
23    A  No, I have not.                  11:46
24      MR. SHEASBY:  I pass the witness.          11:46
25      MS. FINN:  Sorry.  Let's take just a        11:46
```

22 (Pages 82 - 85)

1  five-minute break.                      11:46
2       THE VIDEOGRAPHER:  Thank you.        11:46
3       We're going off the record.  This is the end    11:46
4  of Media Unit 4.  The time is 11:46 a.m.         11:46
5       (Recess taken.)                     11:46
6       THE VIDEOGRAPHER:  We're back on the record.    11:54
7       This is the beginning of Media Unit 5.  The     11:54
8  time is 11:54 a.m.                       11:54
9       MR. RUECKHEIM:  No questions for the Micron     11:54
10  petitioners -- Micron Defendants.  Sorry.        11:54
11      Dr. Stone, thank you for your time.       11:54
12      THE VIDEOGRAPHER:  May I go off the record      11:54
13  for the day, Counsel?                    11:54
14      MR. SHEASBY:  Yes.                  11:54
15      MR. DRYER:  Also, no questions for the       11:54
16  Samsung defendants.                     11:54
17      THE VIDEOGRAPHER:  Thank you very much.       11:54
18      We are off the record at 11:54 a.m., and this   11:54
19  concludes today's testimony given by Dr. Harold Stone.  11:54
20  The total number of media used was five and will be    11:55
21  retained by Veritext Legal Solutions.            11:55
22      (The following was not on the video          11:55
23  recording:)                          11:55
24      MR. SHEASBY:  Can I get a rough of this as      11:55
25  soon as possible?                       11:55

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1  STENOGRAPHIC REPORTER:  Yes.             11:55
2  Counsel, would you like one as well?         11:55
3       MR. RUECKHEIM:  I'll take one as well.     11:55
4       STENOGRAPHIC REPORTER:  And regular        11:55
5  turnaround okay?                        11:55
6       MR. SHEASBY:  No.  I think we need a rush.   11:55
7       STENOGRAPHIC REPORTER:  When would you like   11:55
8  it?                             11:55
9       MR. SHEASBY:  Monday.               11:55
10      STENOGRAPHIC REPORTER:  Sure.          11:55
11      MS. FINN:  Same for Micron.            11:55
12      STENOGRAPHIC REPORTER:  Counsel, would you    11:55
13  like it expedited?                      11:55
14      MR. RUECKHEIM:  Yeah, I'll take whatever    11:55
15  Jason says.                          11:57
16      (WHEREUPON, the deposition ended          11:57
17      at 11:57 a.m.)                      11:57
18           ---oOo---              12:36
19                         12:36
20
21
22
23
24
25

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1      CERTIFICATE OF STENOGRAPHIC REPORTER
2
3      I, ANDREA M. IGNACIO, hereby certify that the
4  witness in the foregoing remote deposition was by me
5  sworn to tell the truth, the whole truth, and nothing
6  but the truth in the within-entitled cause;
7      That said remote deposition was taken in
8  shorthand by me, a disinterested person, at the time
9  and place therein stated, and that the testimony of
10  the said witness was thereafter reduced to
11  typewriting, by computer, under my direction and
12  supervision;
13      That before completion of the deposition,
14  review of the transcript [ ] was [x] was not
15  requested.  If requested, any changes made by the
16  deponent (and provided to the reporter) during the
17  period allowed are appended hereto.
18      I further certify that I am not of counsel or
19  attorney for either or any of the parties to the said
20  deposition, nor in any way interested in the event of
21  this cause, and that I am not related to any of the
22  parties thereto.
23  Dated: August 20, 2023
24
25  ANDREA M. IGNACIO, RPR, CRR, CCRR, CLR, CSR No. 9830

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1  Mr. Jason Sheasby, Esq.
2  jsheasby@irell.com
3              August 20, 2023
4  RE: NETLIST, INC. vs. SAMSUNG ELECTRONICS CO, LTD
5  August 18, 2023, Harold S. Stone, Ph.D. (JOB NO. 6045577)
6  The above-referenced transcript has been
7  completed by Veritext Legal Solutions and
8  review of the transcript is being handled as follows:
9  __ Per CA State Code (CCP 2025.520 (a)-(e)) – Contact Veritext
10    to schedule a time to review the original transcript at
11    a Veritext office.
12  __ Per CA State Code (CCP 2025.520 (a)-(e)) – Locked .PDF
13    Transcript - The witness should review the transcript and
14    make any necessary corrections on the errata pages included
15    below, notating the page and line number of the corrections.
16    The witness should then sign and date the errata and penalty
17    of perjury pages and return the completed pages to all
18    appearing counsel within the period of time determined at
19    the deposition or provided by the Code of Civil Procedure.
20  __ Waiving the CA Code of Civil Procedure per Stipulation of
21    Counsel - Original transcript to be released for signature
22    as determined at the deposition.
23  __ Signature Waived – Reading & Signature was waived at the
24    time of the deposition.
25

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23 (Pages 86 - 89)

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 1  __ Federal R&S Requested (FRCP 30(e)(1)(B)) – Locked .PDF
 2   Transcript - The witness should review the transcript and
 3   make any necessary corrections on the errata pages included
 4   below, notating the page and line number of the corrections.
 5   The witness should then sign and date the errata and penalty
 6   of perjury pages and return the completed pages to all
 7   appearing counsel within the period of time determined at
 8   the deposition or provided by the Federal Rules.
 9  _X_ Federal R&S Not Requested - Reading & Signature was not
10    requested before the completion of the deposition.
11
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 1  NETLIST, INC. vs. SAMSUNG ELECTRONICS CO, LTD
 2  Harold S. Stone, Ph.D. (JOB NO. 6045577)
 3           E R R A T A  S H E E T
 4  PAGE_____ LINE_____ CHANGE_____
 5  _____
 6  REASON_____
 7  PAGE_____ LINE_____ CHANGE_____
 8  _____
 9  REASON_____
10  PAGE_____ LINE_____ CHANGE_____
11  _____
12  REASON_____
13  PAGE_____ LINE_____ CHANGE_____
14  _____
15  REASON_____
16  PAGE_____ LINE_____ CHANGE_____
17  _____
18  REASON_____
19  PAGE_____ LINE_____ CHANGE_____
20  _____
21  REASON_____
22
23  _____  _____
24  WITNESS                    Date
25
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| **11**  76:25 77:7,9 |
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Federal Rules of Civil Procedure

Rule 30

(e)  Review By the Witness; Changes.

(1)  Review; Statement of Changes. On request by the deponent or a party before the deposition is completed, the deponent must be allowed 30 days after being notified by the officer that the transcript or recording is available in which:

(A)  to review the transcript or recording; and

(B)  if there are changes in form or substance, to sign a statement listing the changes and the reasons for making them.

(2)  Changes Indicated in the Officer's Certificate. The officer must note in the certificate prescribed by Rule 30(f)(1) whether a review was requested and, if so, must attach any changes the deponent makes during the 30-day period.

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